UNIVERSITY OF LIVERPOOL

Experiment 5 - Design of an operational Amplifier Using PSpice

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Abstract

This report discussed the design of an operating amplifier meeting certain specifications. The configuration design explanation, detailed calculation process, different schematics drawn in PSpic, and the simulation procedure and results were all presented in this report. The designed amplifier has generally met all the expected requirements and could perform as a proper amplifier as has been simulated.

The DC sweep, transient mode, and AC sweep were used in the procedure of conducting the simulation using PSpice. The frequency response with or without a compensation capacitor and its common-mode signal amplification feature have been examined as well, which help understand the related professional knowledge of frequency response. Error analysis on the slight difference between the theoretical results of parameters and the experimental simulation results has been conducted.

Concretely, this designed amplifier has a voltage gain with magnitude of around 13,000,000, with a high input impedance around $140k\Omega$ and a low output impedance no bigger than $1k\Omega$. Its bandwidth with a compensation capacitor was found out to be around 25.119Hz, and its offset DC voltage required was obtained to be around $-107.111\mu V$.

Declaration

I confirm that I have read and understood the Universitys definitions of plagiarism and collusion from the Code of Practice on Assessment. I confirm that I have neither committed plagiarism in the completion of this work nor have I colluded with any other party in the preparation and production of this work. The work presented here is my own and in my own words except where I have clearly indicated and acknowledged that I have quoted or used figures from published or unpublished sources (including the web). I understand the consequences of engaging in plagiarism and collusion as described in the Code of Practice on Assessment (Appendix L).

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1 Introduction

1.1 Background

Operational amplifier (op-amp) is one of the most essential and widely used electronic devices in the modern world, which is mainly due to its feature that its characteristics can be independent from its only manufacturing variation but depend on external components with the existence of negative feedback [1]. Op-amp is the type of amplifier that has high voltage gain, differential input and a single-ended output as can be seen in Figure 1.

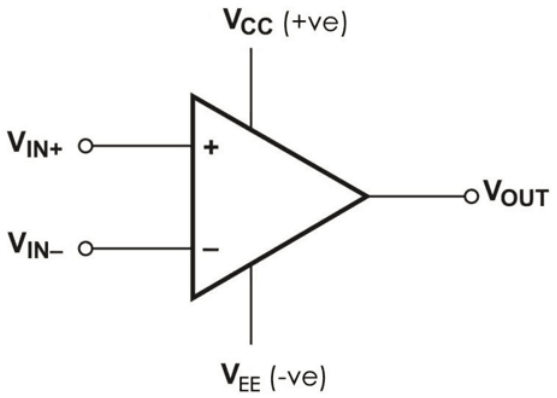

Figure 1: Conceptual graph for an operational amplifier

1.2 Objective

An operating amplifier should be designed and built with the aid of PSpice. The design specifications can be seen in the Table 1 below.
To complete this design, it was expected that the amplifier should be composed of different stages learnt from module ELEC 271. Also, the problems and challenges met during the process should be aware of and discussed.

Table 1: Design Specification

Concrete parameter expected values
differential input impedance no less than $100k\Omega$
voltage gain greater than 500,000
output impedance no bigger than $1k\Omega$
output voltage approximates zero for zero input
frequency response down to zero (DC)
supply voltage is from -9V to 9V
total current consumption is no bigger than 5mA

1.3 Theory

1.3.1 Different components properties

Common emitter (CE) and emitter follower (EF): The output load is connected to the collector of CE or the emitter of EF, this is a method to distinguish these two configurations [2]. The voltage gain of CE is high while that of EF is low since EF is usually used to match impedance rather than amplify voltage.
Current mirror: The core configuration feature is that two bases are connected together which enable the two collector currents to be virtually the same [3].
Differential amplifier: A differential amplifier can only amplify the difference of the two signals but if the two inputs are common-mode, the differential amplifier will not function [2].
Early voltage: The early voltage, an important parameter which would be used in the calculation of the resistances can be obtained based on the characteristics curve of a transistor as can be seen in Figure 2 below [4]. Particularly, in this design, the early voltage values used are 116(pnp) and 72(npn) respectively.

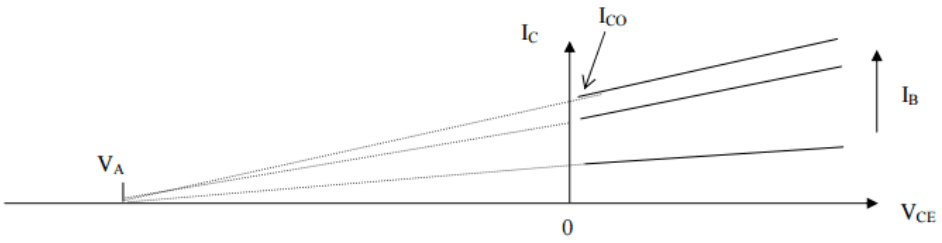

Figure 2: To obtain early voltage

1.3.2 Circuit configuration explanation

Four blocks are included in this design of the configuration, which are emitter follower, common emitter, current mirror circuit, and differential input stage. The whole circuit has five stages as shown in Figure 3 achieving four purposes.
Stage one sets the DC bias for all the following stages in this designed circuit. Stage two and four provide high voltage gain. Stage three matches the gain stage to avoid loading effects. Stage five provides low output resistance [5].

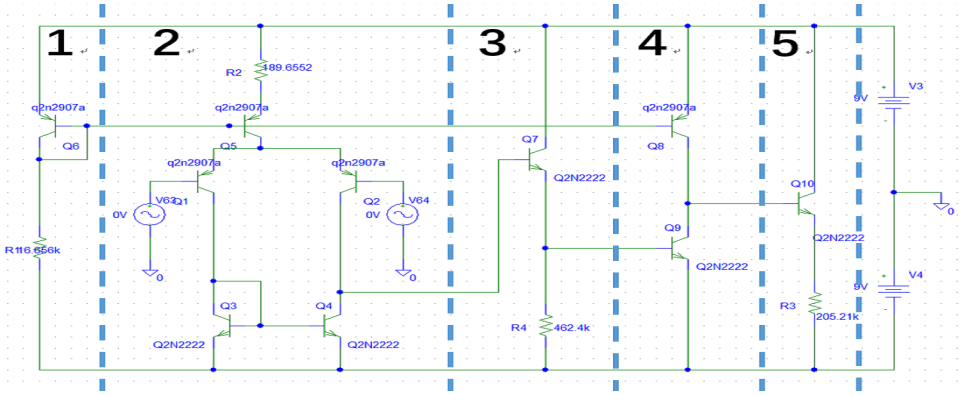

Figure 3: Five stage version of schematics

2 Materials and Methods

2.1 Calculation

2.1.1 Method one (the adopted method)

This section is based on the assumption of $V_{R2} = 0.04V$, $R_{OUT} = 800\Omega$, and $R_{id} = 110000\Omega$ (This assumption was obtained from a program written based on this calculation procedure which will discussed in the following section).

- $\boldsymbol{R_2}$

According to properties of differential amplifier, we know that $R_{id} = 2r_{be}$, and $r_{be} = \frac{\beta}{I_C}$, which together give the equation below:

$$R_{id} = 2r_{be} = \frac{2 \times \beta_{o(npn)}}{40 \times I_{C1}} = 120k\Omega \tag{1}$$

Since Q1 and Q2 apparently constitute a current mirror, we can further derive equations below:

$$I_{C1} = I_{C2} = \frac{1}{2} I_{C5} \tag{2}$$

$$I_{C5} = \frac{\beta_{pnp}}{(10 \times R_{id})} = 2.1091 \times 10^{-4} A \tag{3}$$

$$R_2 = \frac{V_{R2}}{I_{C5}} = 189.6552\Omega \tag{4}$$

We obtain $R_2 = 189.6552\Omega$.

- $\boldsymbol{R_1}$

It can be seen clearly that Q5 and Q6 constitute a widlar current mirror, whose property derives equation below:

$$R_E \times I_O = V_T \times ln(\frac{I_{ref}}{I_O}) \tag{5}$$

While in this case, $R_E = R_2$, $I_{ref} = I_{C6}$, $I_O = I_{C5}$, equation below can be derived:

$$R_2 \times I_{C5} = V_T \times ln(\frac{I_{C6}}{I_{C5}}) \tag{6}$$

$$I_{C6} = I_{C5} \times e^{\frac{(R2 \times I_{C5})}{V_T}} = 0.001V \tag{7}$$

$$R_1 = \frac{(V_{CC} - V_{EE} - V_{BE})}{I_{C6}} = 16.656k\Omega \tag{8}$$

We obtain $R_1 = 16.656k\Omega$.

• $\boldsymbol{R_4}$ and $\boldsymbol{R_3}$

Several parameters were calculated first for following calculation:

$$r_{ce2} = \frac{V_{A(pnp)}}{(I_{C5}/2)} = 1100000\Omega \tag{9}$$

$$r_{ce4} = \frac{V_{A(npn)}}{(I_{C5}/2)} = 6.8276 \times 10^5\Omega \tag{10}$$

$$r_{be9} = \frac{\beta_{npn}}{(I_{C6} \times 40)} = 4.2838 \times 10^3\Omega \tag{11}$$

$$r_{ce8} = \frac{V_{A(pnp)}}{I_{C6}} = 1.1104 \times 10^5\Omega \tag{12}$$

$$r_{ce9} = \frac{V_{A(npn)}}{I_{C6}} = 6.8923 \times 10^4\Omega \tag{13}$$

$$r_{ce2}||r_{ce4} = \frac{r_{ce2} \times r_{ce4}}{r_{ce2} + r_{ce4}} = 4.2128 \times 10^5\Omega \tag{14}$$

$$r_{ce8}||r_{ce9} = \frac{r_{ce8} \times r_{ce9}}{r_{ce8} + r_{ce9}} = 4.2527 \times 10^4\Omega \tag{15}$$

The output resistance of the differential amplifier is:

$$R_{IN(CC)} = 10 \times R_{OUT(DA)} \tag{16}$$

The left hand side and right hand side parameters can be expressed:

$$R_{OUT(DA)} = r_{ce(2)}||R_{ce(4)} \tag{17}$$

$$R_{IN(CC)} = r_{be(7)} + (1 + \beta_o)R_E||r_{be(9)} \tag{18}$$

Also, the current I_{C7} which is required to work out r_{ce7} can be obtained:

$$V_{BE} = I_{C7} \times R_4 \tag{19}$$

The equation containing only one unknown parameter R_4 is:

$$\frac{\beta_{npn} \times R_4}{(40 \times V_{BE})} + (\beta_{npn} + 1) \times \frac{R_4 \times r_{be9}}{(R_4 + r_{be9})} = 10 \times r_{ce2}||r_{ce4} \tag{20}$$

The equation containing only one unknown parameter R_3 is:

$$R_{OUT} = (\frac{r_{be(10)} + r_{be(8)}||r_{be(9)}}{\beta_o})||R_3 = 800\Omega \tag{21}$$

We obtain $R_4 = 462.4k\Omega$, and $R_3 = 205.21k\Omega$.

Programmable process of the adopted method
The calculation process in a programmable logic can be written as below. The Matlab function code whose inputs are the three assumptions is in Appendix B.

Assumption

$V_{R2} = 0.04V$

$R_{id} = 110k\Omega$

$V_{OUT} = 800V$

Known Parameters

$V_{CC} = 9V$

$V_{EE} = -9V$

$V_{BE} = 0.6V$

$V_T = 0.025V$

$V_{A(npn)} = 72V$

$V_{A(pnp)} = 116V$

$\beta_{npn} = 179$

$\beta_{pnp} = 232$

Calculation Procedure

$I_{C5} = \beta_{pnp}/10/R_{id}$

For R_2**:** $R_2 = V_{R2}/I_{C5}$

$I_{C6} = I_{C5} \times e^{(R_2 \times I_{C5}/V_T)}$

For R_1**:** $R_1 = (V_{CC} - V_{EE} - V_{BE})/I_{C6}$

$r_{ce2} = V_{A(pnp)}/(I_{C5}/2)$

$r_{ce4} = V_{A(npn)}/(I_{C5}/2)$

$r_{be9} = \beta_{npn}/(I_{C6} \times 40)$

$r_{ce8} = V_{A(pnp)}/I_{C6}$

$r_{ce9} = V_{A(npn)}/I_{C6}$

$A = r_{ce2} \times r_{ce4}/(r_{ce2} + r_{ce4})$

$B = \beta_{npn} + 1$

$C = r_{ce8} \times r_{ce9}/(r_{ce8} + r_{ce9})$

For R_3**:** $((C + \beta_{npn} * R_3/(40 \times 9))/B) \times R_3/(R_3 + ((C + \beta_{npn} \times R_3/(40 \times 9))/B)) = V_{OUT}$

For R_4**:** $\beta_{npn} \times R_4/(40 \times V_{BE}) + B \times (R_4 \times r_{be9}/(R_4 + r_{be9})) = 10 \times A$

Usage of the program
Different assumptions were used as the inputs of this function, the resulting resistances were applied on the schematics and their simulation results such as the output impedance was observed. After trails and errors, a proper group of values of those assumed parameters were obtained as that have been used in previous section.

2.1.2 Method two

There is also an alternative method of calculation which starts the assumption from the I_{C6}, and the value of I_{C6} is usually assumed to be $1mA$.
This method should be reasonable as well since the total consumption of current should be no bigger than $5mA$ and there are five lines of paths totally in the designed circuit.

• $\boldsymbol{R_1}$

The R_1 is first worked out based on the voltage division theory.

$$R_1 = \frac{V_{CC} + V_{EE} - V_{BE}}{I_{C6}} = \frac{9 + 9 - 0.6}{1} = 17.4k\Omega \tag{22}$$

• $\boldsymbol{R_2}$

According to properties of differential amplifier, we know that $R_{id} = 2r_{be}$, and $r_{be} = \frac{\beta}{I_C}$, which together derive equation below:

$$R_{id} = 2r_{be} = \frac{2 \times \beta_{o(npn)}}{40 \times I_{C1}} = 120k\Omega \tag{23}$$

Since Q1 and Q2 apparently constitute a current mirror, we can further derive equation (3). We obtain $I_{C5} = 0.2083mA$.

$$I_{C1} = I_{C2} = \frac{1}{2} I_{C5} \tag{24}$$

It can be seen clearly that Q5 and Q6 constitute a widlar current mirror, whose property derives equation below:

$$R_E \times I_O = V_T \times ln(\frac{I_{ref}}{I_O}) \tag{25}$$

While in this case, $R_E = R_2$, $I_{ref} = I_{C6}$, $I_O = I_{C5}$, based on which, equation below can be derived. We can obtain R_2 using it.

$$R_2 \times I_{C5} = V_T \times ln(\frac{I_{C6}}{I_{C5}}) \tag{26}$$

Comment
The only difference between this method and the method adopted in this design is that the order of calculating R_1 and R_2 is switched. While for R_3 and R_4, the procedure is the same. The calculation process of R_1 and R_2 is presented below and it can be seen clearly that the obtained values are not so different from the values obtained using the adopted method.

2.2 Procedure

2.2.1 Part I

The circuit for obtaining the I-V characteristics for transistor can be shown in Figure 4. The left one is for NPN and the right is for PNP. The difference is the direction of the sources.

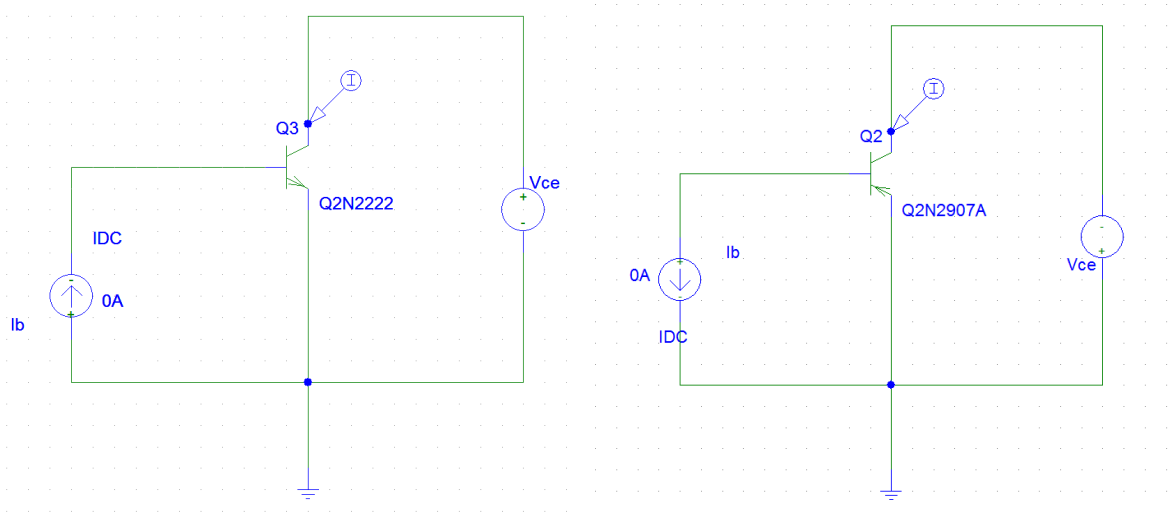

Figure 4: circuit for NPN and PNP

This is because to turn on a NPN transistor, the gate voltage requires a positive value bigger than threshold voltage, while to turn on a PNP transistor, the gate voltage requires a negative value with absolute magnitude bigger than the threshold voltage.

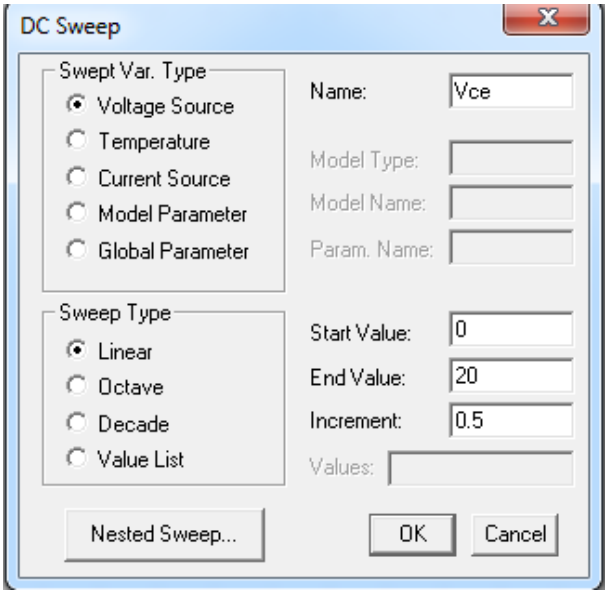

Figure 5: Setup window

To run the simulation, the analysis botton in toolbar was pressed and the DC sweep mode was chosen, the detailed setup parameters can be seen in Figure 5.

2.2.2 Part II task 2,3,4

The circuit is shown in Figure 6 where the source used is VSCR type, and the DC sweep mode was chosen and the detailed setup parameters can be seen in Figure 7.

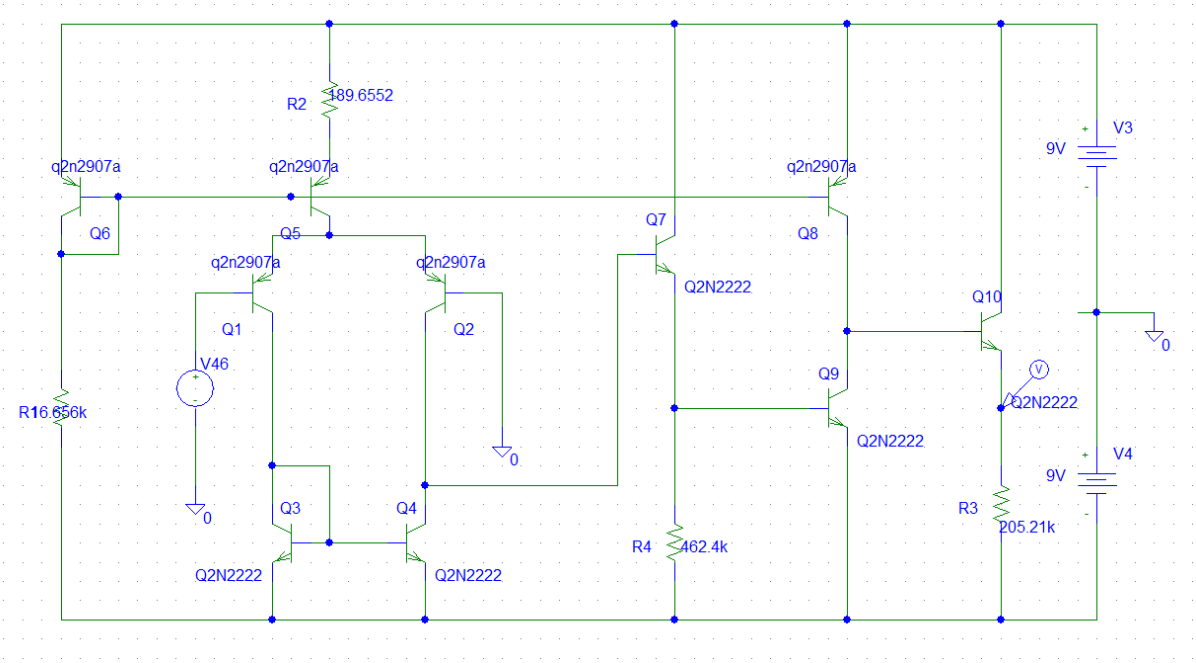

Figure 6: circuit with VSCR source

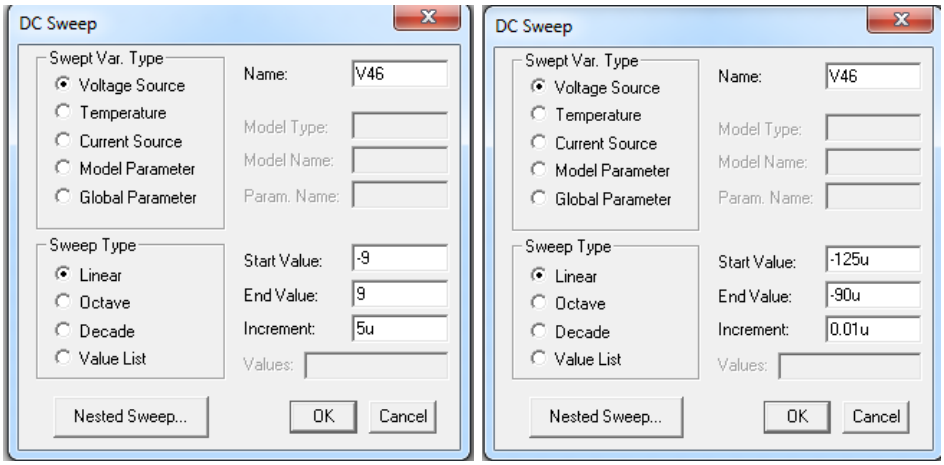

Figure 7: Set up

2.2.3 Part II task 5

The circuit for task 5 is shown in Figure 8 where the source used is VSIN type, and the transient sweep mode was chosen and the detailed setup parameters can be seen in Figure 9.

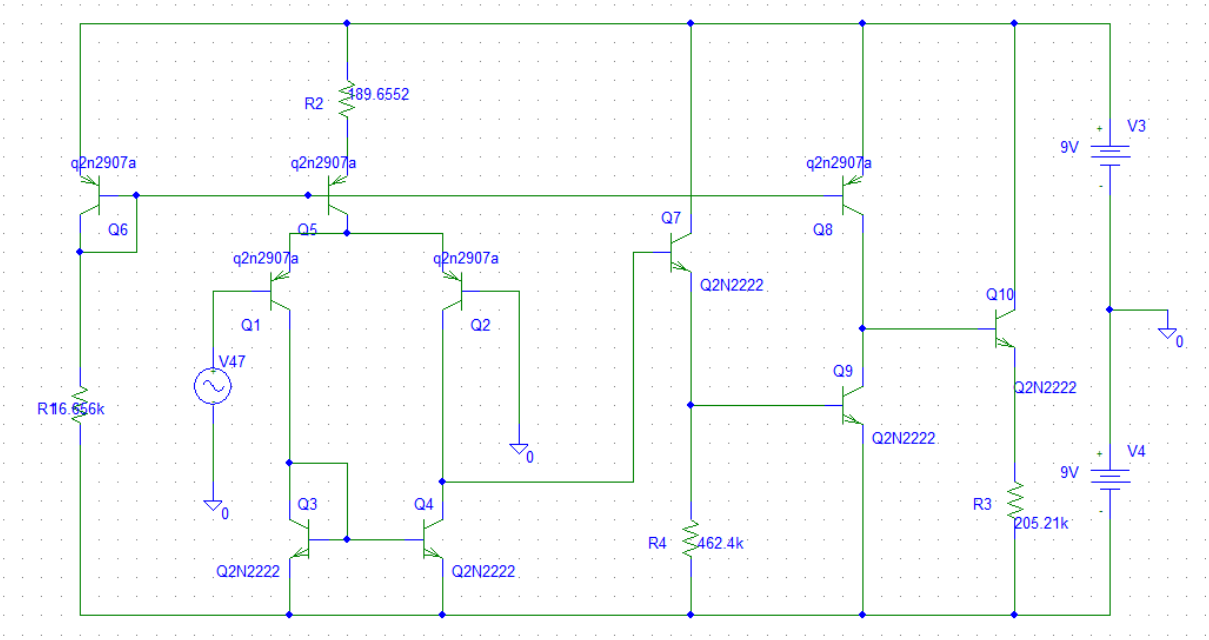

Figure 8: circuit with VSIN source

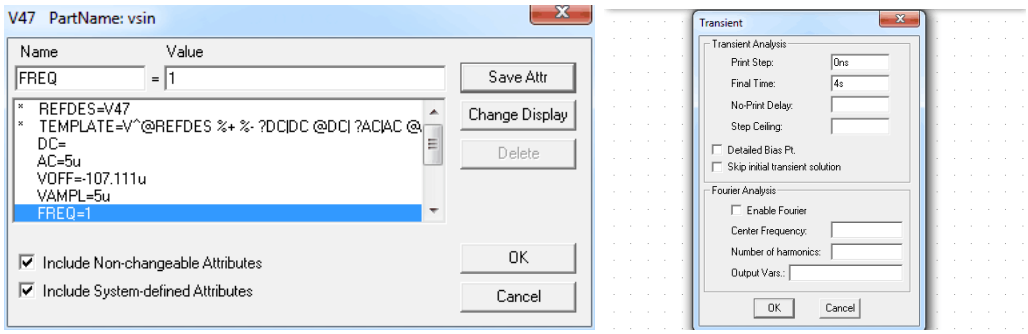

Figure 9: Set up

The amplitude of the VSIN source V47 in Figure was changed to 9V and $10/muV$ as well to show the simulation result of too large range of voltage range as comparison with the required result, the simulation graphs of which can be seen in Appendix A.

2.2.4 Part II task 6

The circuit for obtaining input impedance is shown in Figure 10 where the source used is VSIN type, and the AC sweep mode was chosen and the detailed setup parameters can be seen in Figure 11.

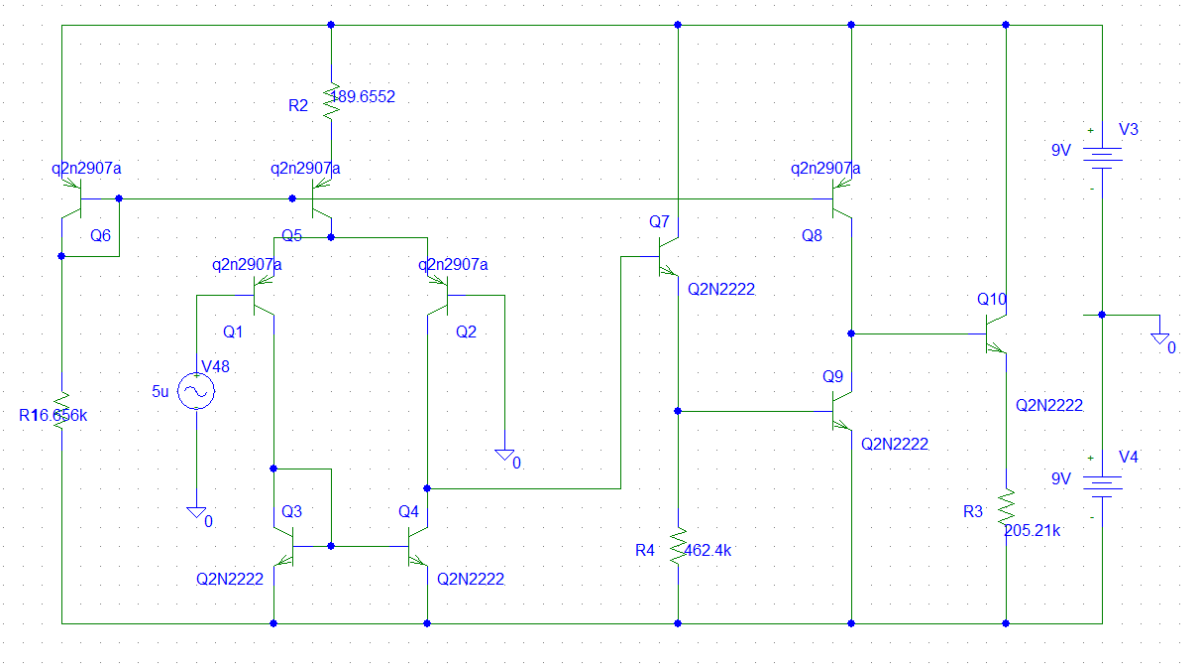

Figure 10: Circuit for obtaining input impedance

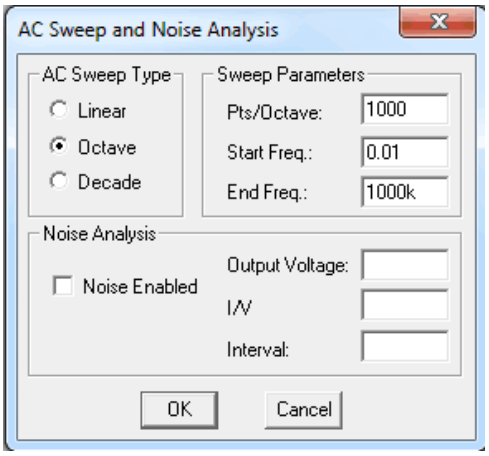

Figure 11: Circuit for obtaining input impedance

The impedance trace added was $V(Q1b)/I(Q1b)$ since the input impedance seen from the input should be the base voltage over base current of the Q1 transistor that directed connected to the source.

The circuit for obtaining output impedance is shown in Figure 12 where the source used is VSIN type, and the AC sweep mode was chosen and the detailed setup parameters can be seen in Figure 11.

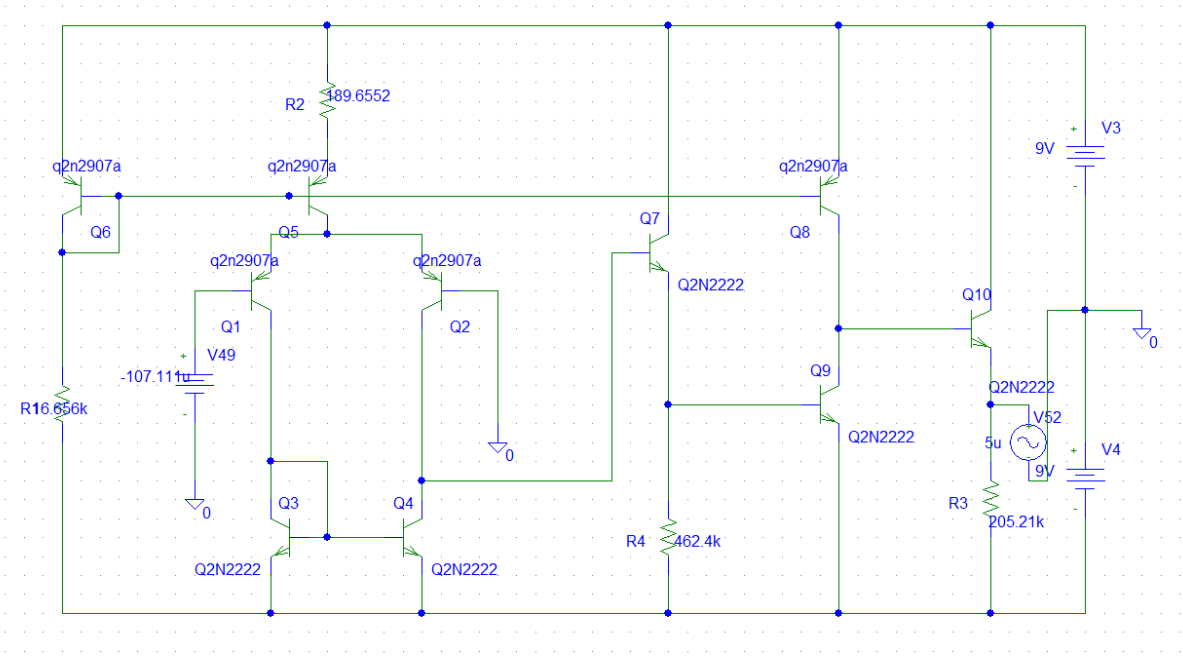

Figure 12: Circuit for obtaining output impedance

The impedance trace added was $V1(V52)/I1(V52)$ since the input impedance seen from the output should be the Thevenin voltage over the current of the short circuit current when the input source is short circuited.

2.2.5 Part III task 1

The circuit for obtaining frequency response is shown in Figure 13 where the source used is VAC type, and the AC sweep mode was chosen and the detailed setup parameters can be seen in Figure 14.

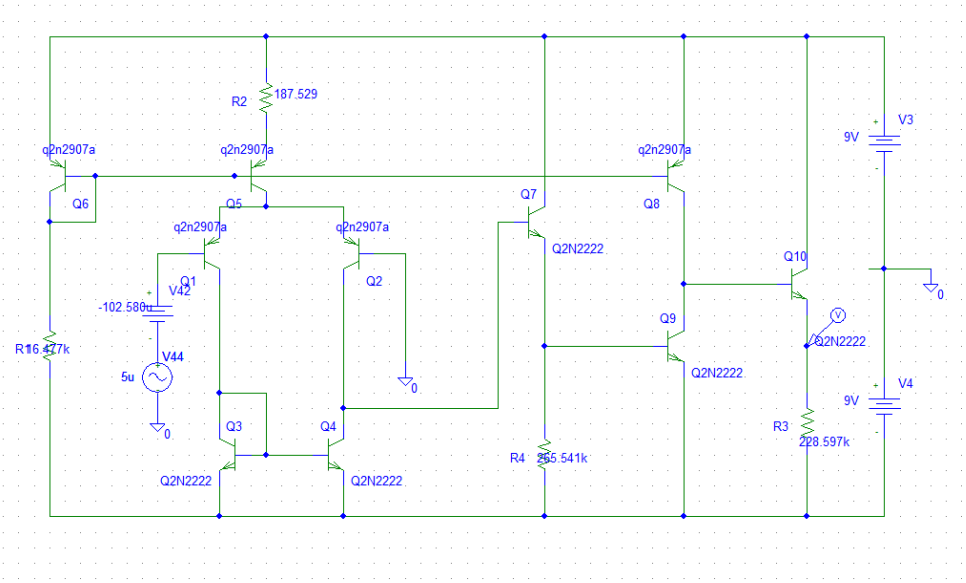

Figure 13: Circuit without the capacitor

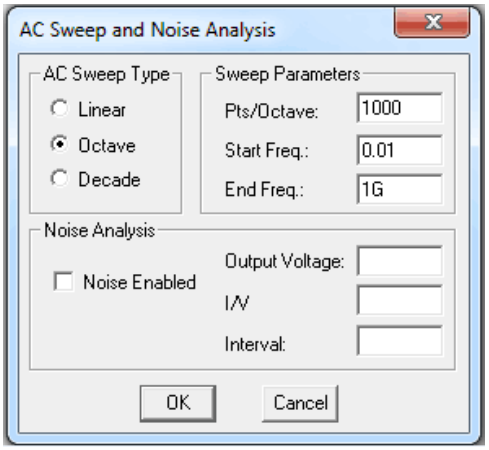

Figure 14: Setup window

The trace added was $DBV(Q10e)/V(Q1b)$ and $PV(Q10e)/V(Q1b)$ which demonstrate the gain amplitude in decibel form and the phase of it respectively.

2.2.6 Part III task 2

The circuit for frequency response with a compensation capacitor added is shown in Figure 15 where the source used is VAC type, and the AC sweep mode was chosen and the detailed setup parameters can be seen in Figure 14.

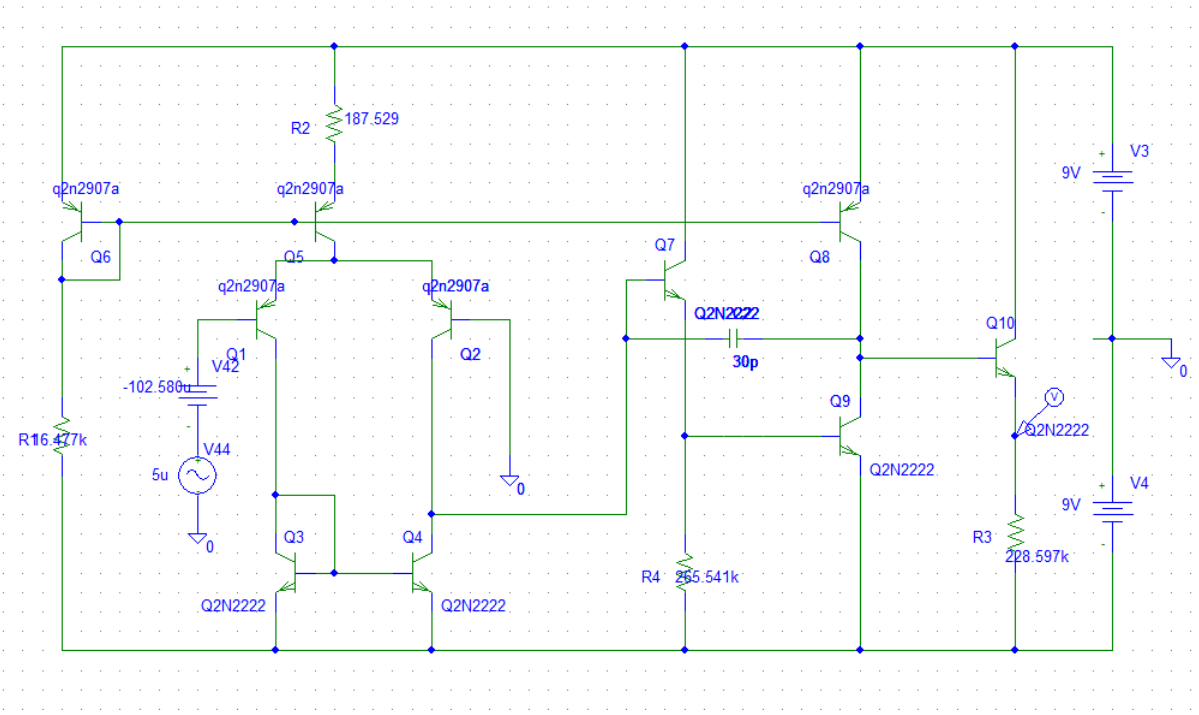

Figure 15: circuit with the capacitor

The impedance trace added was the same as task 1 since the only difference between these two tasks was the addition of the compensation capacitor.

2.2.7 Bonus

The circuit for obtaining voltage gain with common-mode signal source with and without the compensation capacitor are shown in Figure 16 and Figure 17 respectively where the source used is VSIN type, and the AC sweep mode was chosen and the detailed setup parameters can be seen in Figure 11.

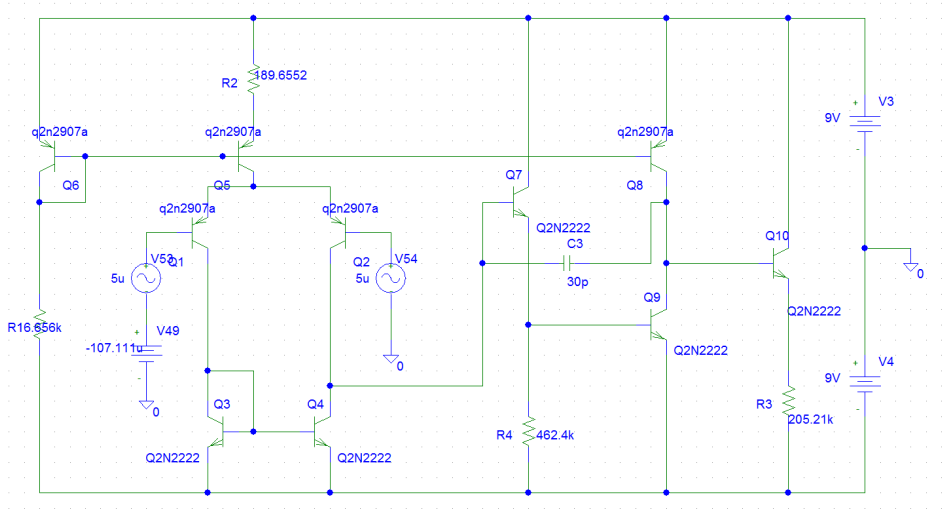

Figure 16: common-mode source

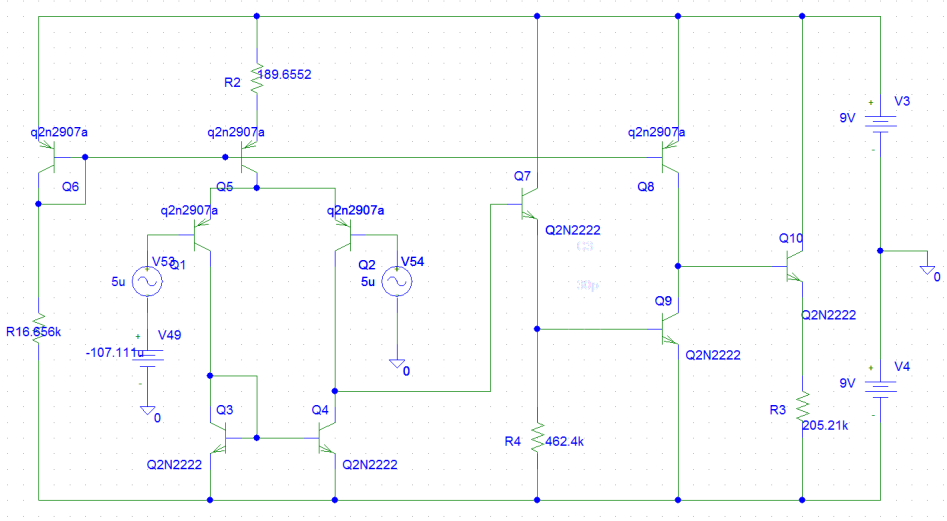

Figure 17: common-mode source and capacitor

The impedance trace added was $V(Q10e)/I(Q1b)$ since the voltage gain of this amplifier should be the Q10 transistor emitter voltage which is the output voltage terminal connected to input source over the Q1 transistor base voltage which is the input voltage terminal connected to the load.

3 Results

3.1 Part one

3.1.1 Task 3 & 4

The AC current gain (NPN and PNP) were approximately obtained using equation $\beta_O = \frac{\Delta I_C}{\Delta I_B}$, which were used in calculation step as discussed in previous section. The simulation graph can be seen in Figure 18 and Figure 19.

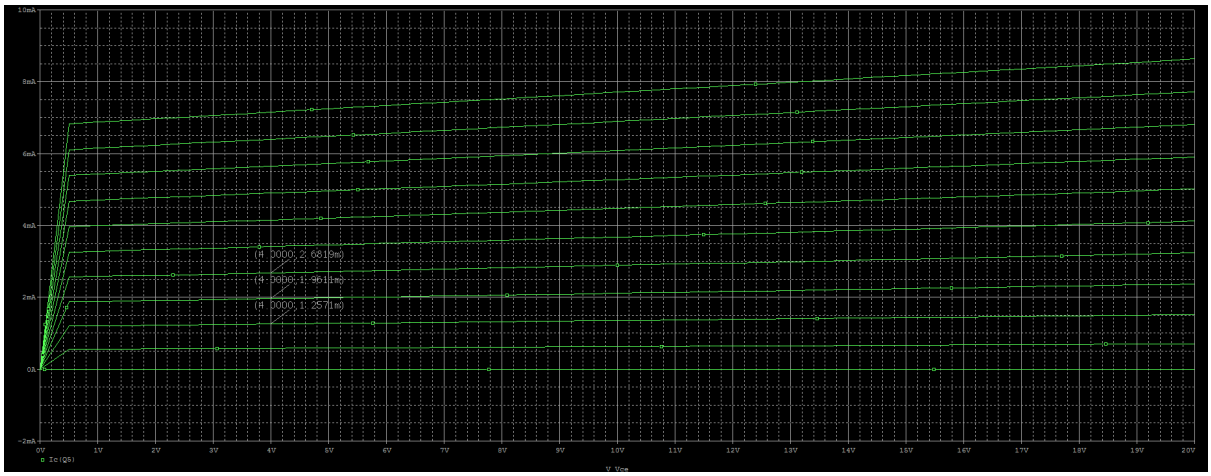

Figure 18: NPN characteristics

$$\beta_{O(NPN)} = \frac{(\frac{2.6819m - 1.9611m}{4\mu} + \frac{1.9611m - 1.2571m}{4\mu})}{2} = \frac{(182.2 + 175.725)}{2} \approx 179 \qquad (27)$$

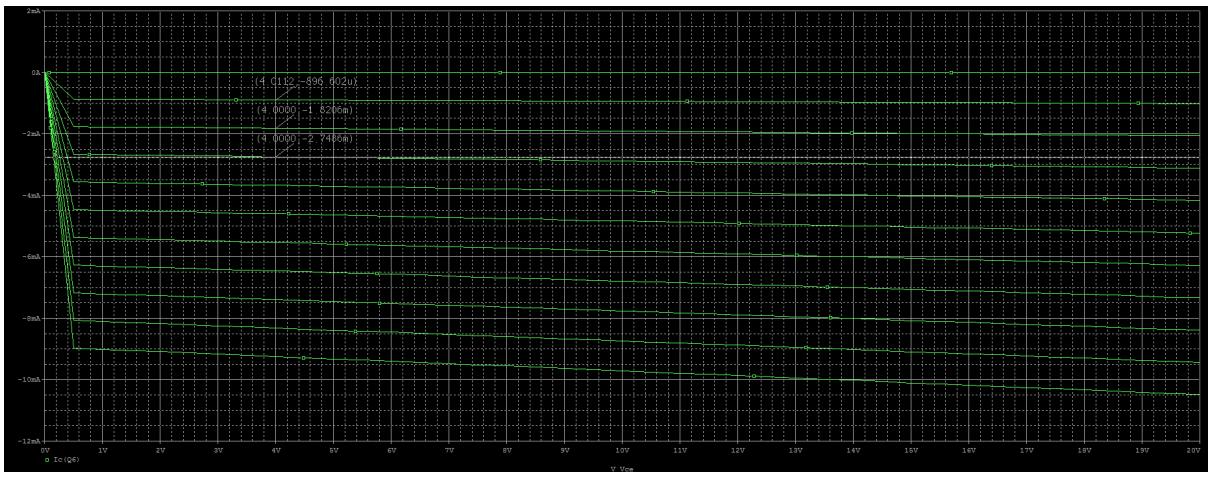

Figure 19: PNP characteristics

$$\beta_{O(NPN)} = \frac{(\frac{-892.602\mu - (-1.8206m)}{4\mu} + \frac{-1.8206m - (-2.7486m)}{4\mu})}{2} = \frac{(231.9995 + 232)}{2} \approx 232 \qquad (28)$$

3.2 Part two

3.2.1 Task 2

The simulation graph for the DC sweep from -9V to 9V is shown in Figure 20.

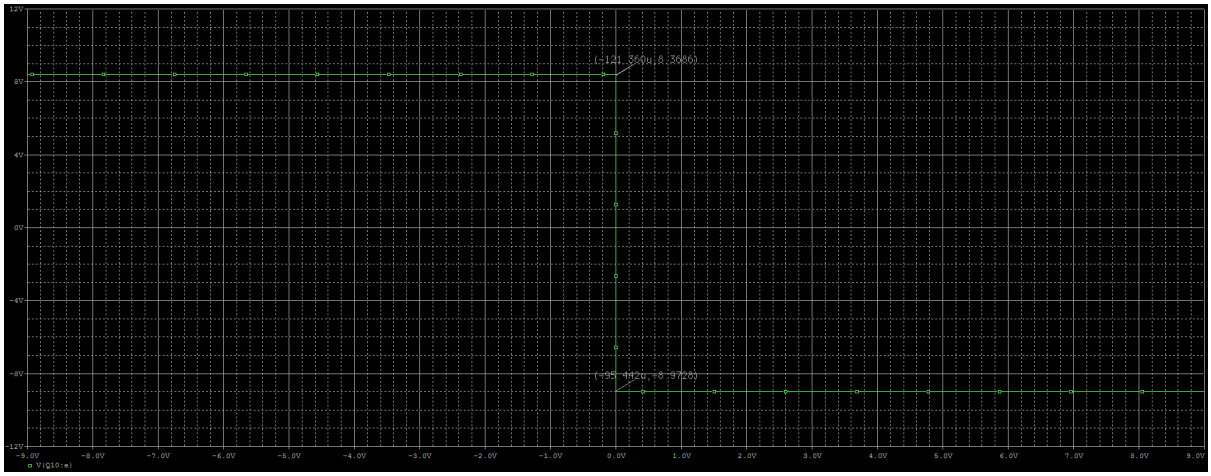

Figure 20: DC sweep from -9V to 9V

It can be seen that the useful operating range should be the slope range. Therefore, the useful range should approximately include the range defined by the horizontal components of the marked two points which is from $-121.360\mu V$ to $-95.442\mu V$. The useful range for source value should be smaller than $6\mu V$.

3.2.2 Task 3

The simulation graph for the DC sweep on narrowed range is shown in Figure 21.

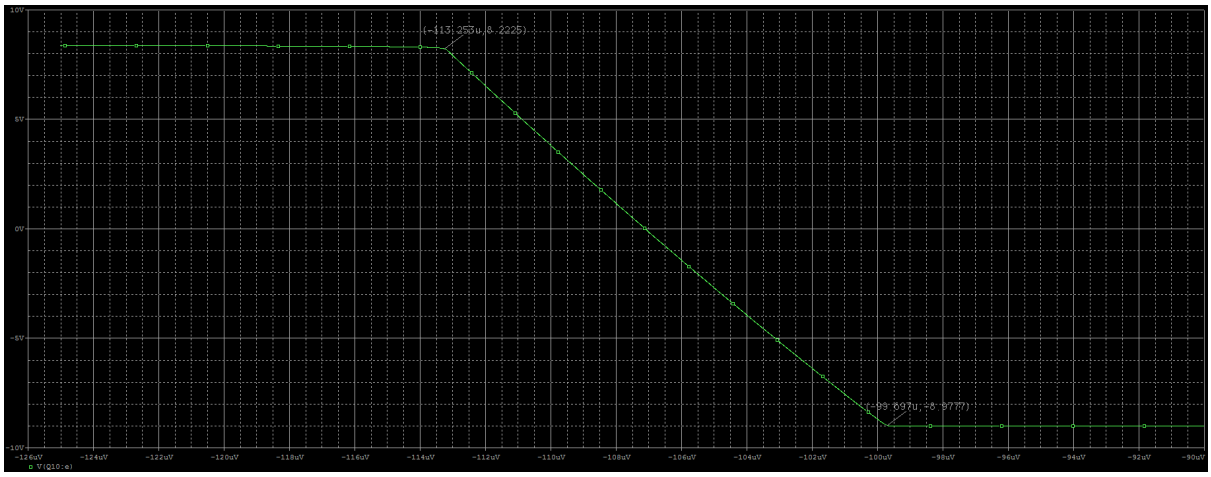

Figure 21: DC sweep for narrowed range

The voltage gain can be worked out using the ratio of the Δy over Δx for the two marked points which are the margin of the useful range. The open-loop gain is the middle region slope of VTC curve. Therefore, $A_V = \frac{8.2225-(-8.9777)}{-113.253\mu-(-99.697\mu)} = -1268825.612$.

3.2.3 Task 4

The marked point in Figure 22 gives the approximate set-off value.

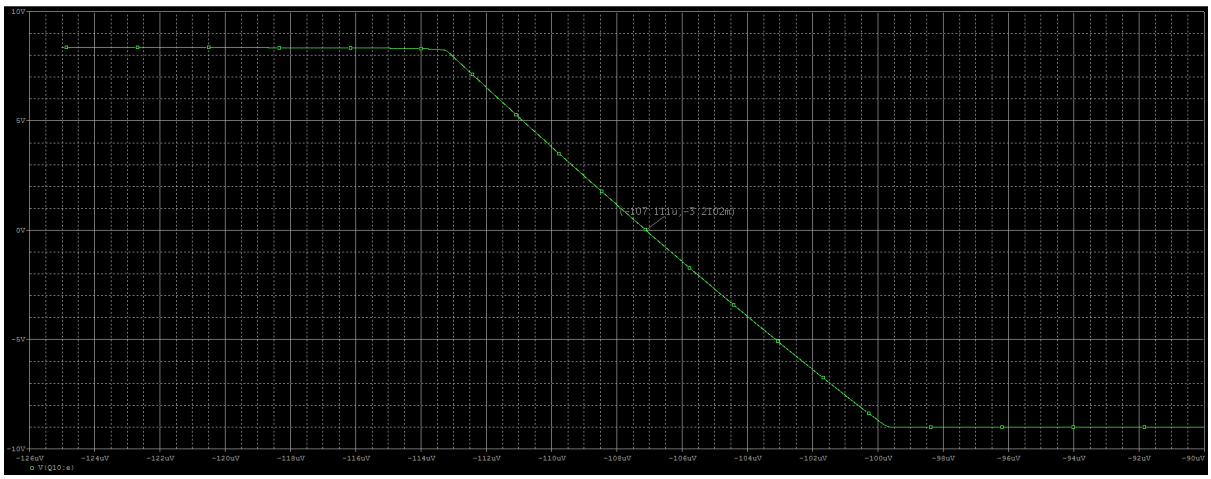

Figure 22: To find the Set-off value

As can be seen in the graph, the vertical component of this point is nearly 0. This means a DC set-off with the value of $-107.111\mu V$, which is the horizontal component of that point, should be applied to balance the amplifier.

3.2.4 Task 5

The simulation graph with VSIN source with amplitude $5\mu V$ is shown in Figure 23.

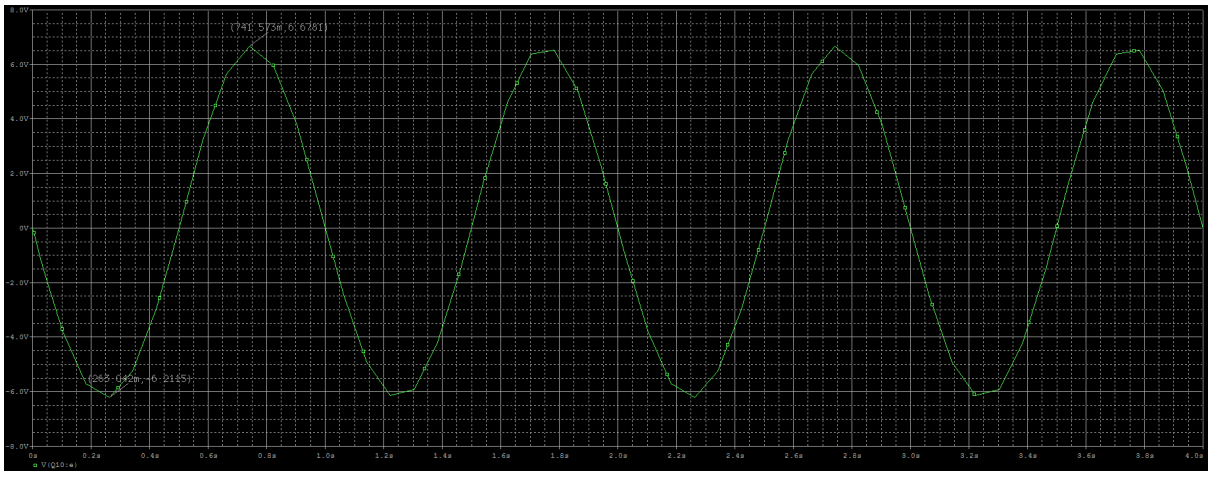

Figure 23: To find the gain value

The voltage gain can be worked out using $A_V = \frac{Maximum - Minimum}{2 \times V_{IN}}$. Therefore, the approximate value can be obtained $A_V = \frac{6.6781 - -6.2115}{2 \times 5\mu} = -1288960$, which apparently meets the specification that the voltage gain should be bigger than 500000 ($1288960 > 500000$).
It was found that as long as the amplitude lies within 6μ, the obtained simulation graph shape were basically the same and the open-loop gain worked out should be quite similar as well. This again verify the conclusion obtained previously, the useful range should be around $6\mu V$.

Also, two simulation graphs for input voltage 9V and $10\mu V$ can be seen in Appendix A which indicates that when the voltage is bigger than $6/muV$, the output will be near to square waveform rather than expected sine waveform since they exceeded the useful range. The simulation graphs are presented below.

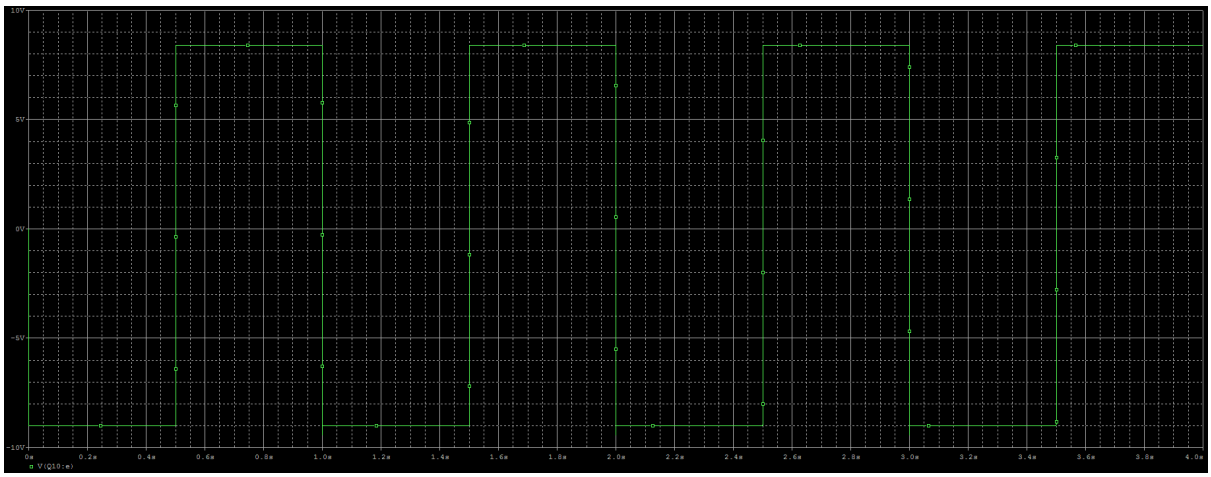

Figure 24: 9V

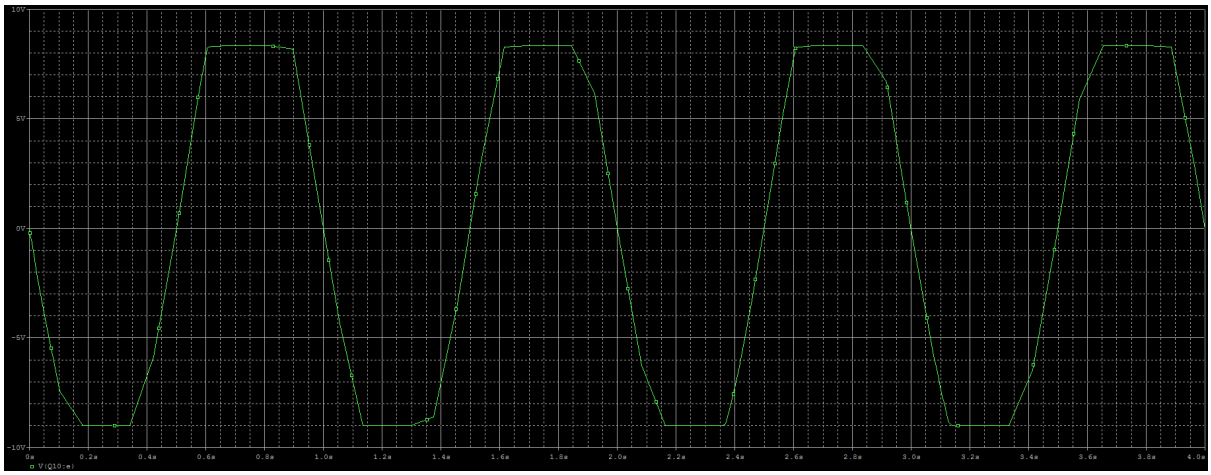

Figure 25: NPN characteristics

It can be observed that when the voltage amplitude of input exceeds the useful range, the gain would be decreased since the expected sine shape curve will be actually clipped off. This make the voltage gain do not meet the expectation of the device and this is the main reason why when we use amplifier we should be careful not to exceed the useful range.
All the scenarios discussed above are based in the fact the the amplitude was changed but the frequency was remained the same. However, if we keep amplitude the same but change the frequency, we will also find that there is a effective frequency for the amplifier to work perfectly. This type of verification and analysis related to the frequency range for amplifier to keep stable gain can be found in the following sections.

3.2.5 Task 6

The simulation graph with with input impedance trace added in the simulation window to indicate the input impedance change in shown in Figure 27.

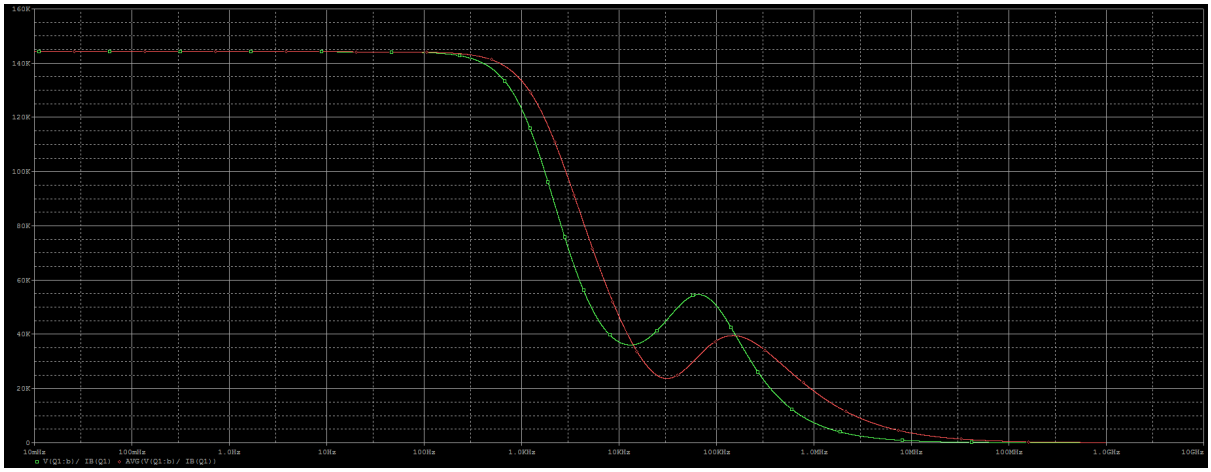

Figure 26: Input impedance

Input impedance of an amplifier is not changed by the amplitude (within the useful range though) or phase of input in a certain frequency range. In the graph above, it can be seen that from 0Hz to 100Hz, the average input impedance remains as a constant with a value of around $145k\Omega$, which is a fairly big value as expected for a proper amplifier that aims at amplifying the voltage.
However, after that range of frequency, the input impedance start to decrease from frequency of 100Hz. It finnaly drops to around zero at the end where the frequency is around 100MHz. Therefore, the amplifier becomes unstable and can not function properly when the frequency under work is too high.

The simulation graph with with output impedance trace added in the simulation window to indicate the output impedance change in shown in Figure 27.

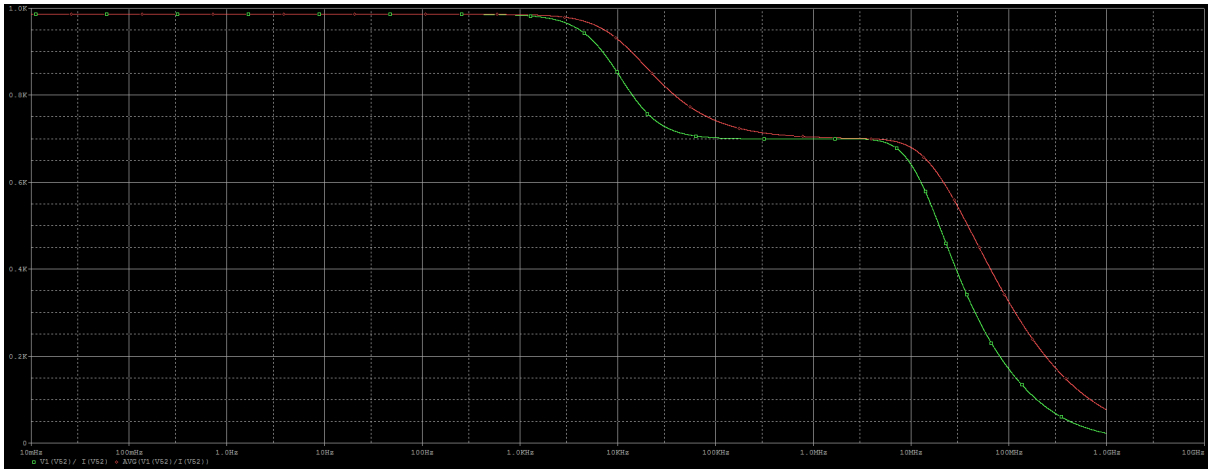

Figure 27: Output impedance

Similarly as how we analysed the graph for input impedance, the output impedance in this graph can be seen is approximately 970Ω and is apparently below $1k\Omega$. This means that the design meets the specification that the output impedance should be no bigger than $1k\Omega$ as mentioned in previous section.
The output impedance is not affected by the input phase and amplitude as long as it does not exceed the useful range as well. However, when the frequency climbs over around 1kHz, the impedance starts to change and finally decrease to virtually zero when the frequency increases to around 1GHz.
Over all, when observing the simulation graphs, we only focus on the low frequency part since within the reasonably low frequency range which should enable the amplifier to function normally. The obvious flat areas of the curves are the effective area whose impedance value should be the value we usually discussed to describe or understand the feature of a amplifier.

3.2.6 Task 7

The simulation graph with all the DC voltage and current values marked is shown in Figure 28.

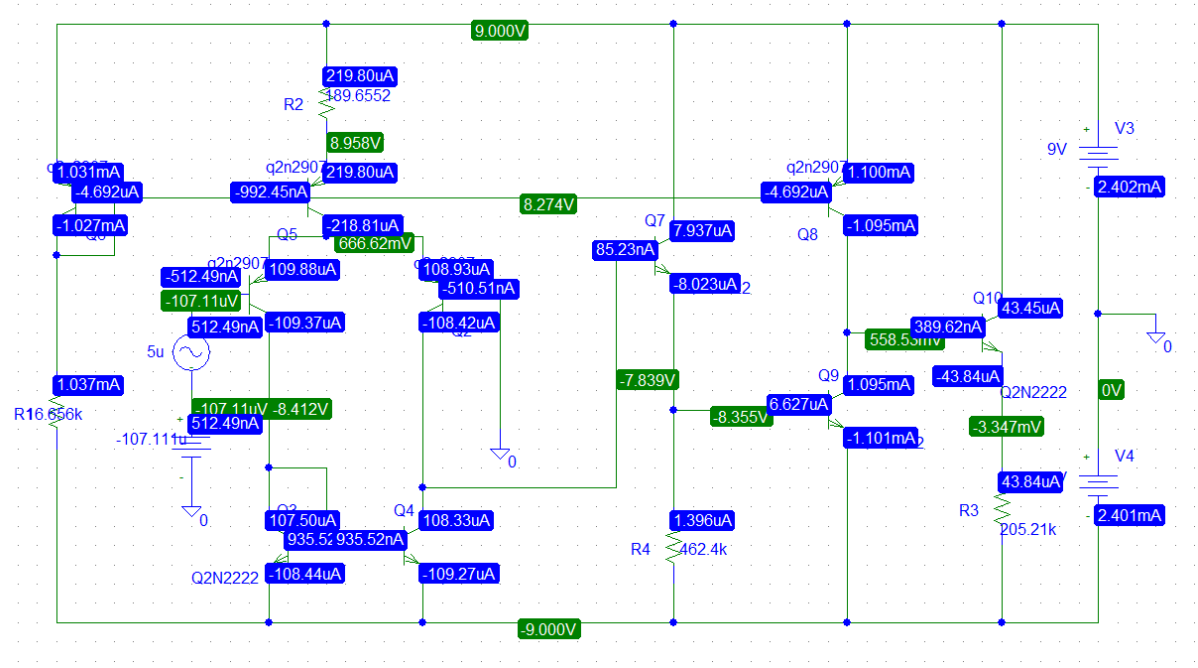

Figure 28: Simulation result with current and voltage value displayed

It can be seen that the DC output voltage is $-3.347mV$ (the green number at the emitter of transistor Q10), which is nearly 0 thus reasonably meeting the specification that the output should be zero.
And the total assumption of current is $2.402mA$ (the blue number at near to the ground), which is much smaller than $5mA$ thus meeting the specification that the total assumption of current should be no bigger than $5mA$.

3.3 Part three

3.3.1 Task 1

The simulation graph for the frequency response is shown in Figure 32, where the phase plot and the gain plot are placed in the same axis system, which is just for the convenience of finding the margin.

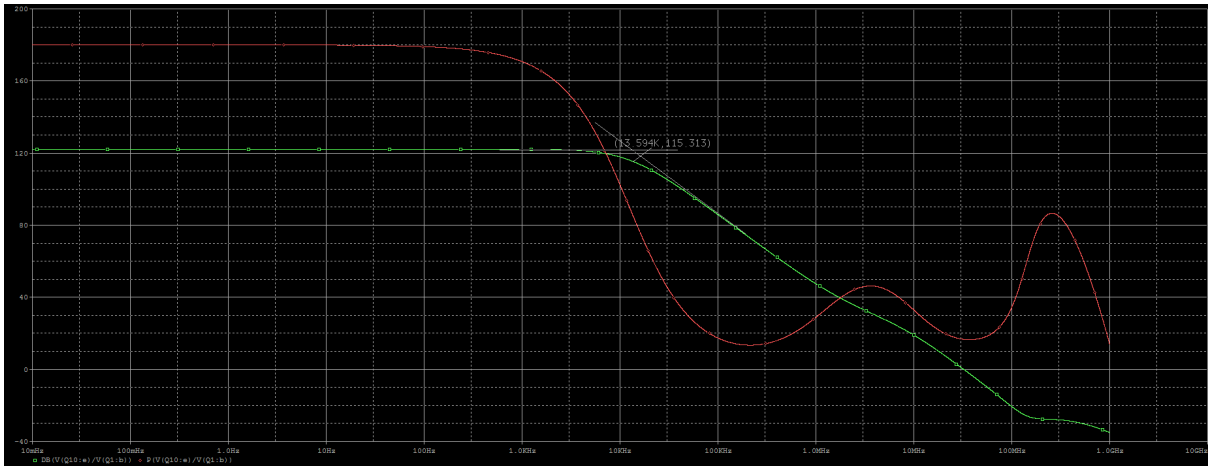

Figure 29: Frequency response without capacitor

Phase margin

The phase margin, which is the vertical components difference between the green curve and the red curve, where the vertical line is drawn across the point where the green curve intersects the 0 response. In this case, the margin is around 18 degree as can be seen in the graph.

As learnt from lectures, the term "margin" means like the required value you should set. In this particular case, the phase margin should be big enough to a certain extent so that the system can be stable.

Bandwidth

Also, for the bandwidth obtained by drawing two tangent lines in the curve frequency part on the gain curve (green curve), the bandwidth is approximately $13.594kHz$ when the gain is reduced by 3dB [6], which is the intersection of the two tangent lines of the gain curve (green curve).

Also, since the bandwidth is defined the corner frequency f_H, there is another method to find the frequency. At this frequency, the gain will be reduced by a factor -3DB or $\frac{1}{\sqrt{2}}$. Therefore, alternatively, we can obtain the frequency by finding the point where the gain in DB form is $A_{ol} - 3DB$ (This will be discussed in detail later in this section).

The DB form gain amplitude plot and the phase plot in different graph without the compensation capacitor added can be seen in Figure below, where the upper graph is for the gain amplitude while the lower one is for the phase plot.

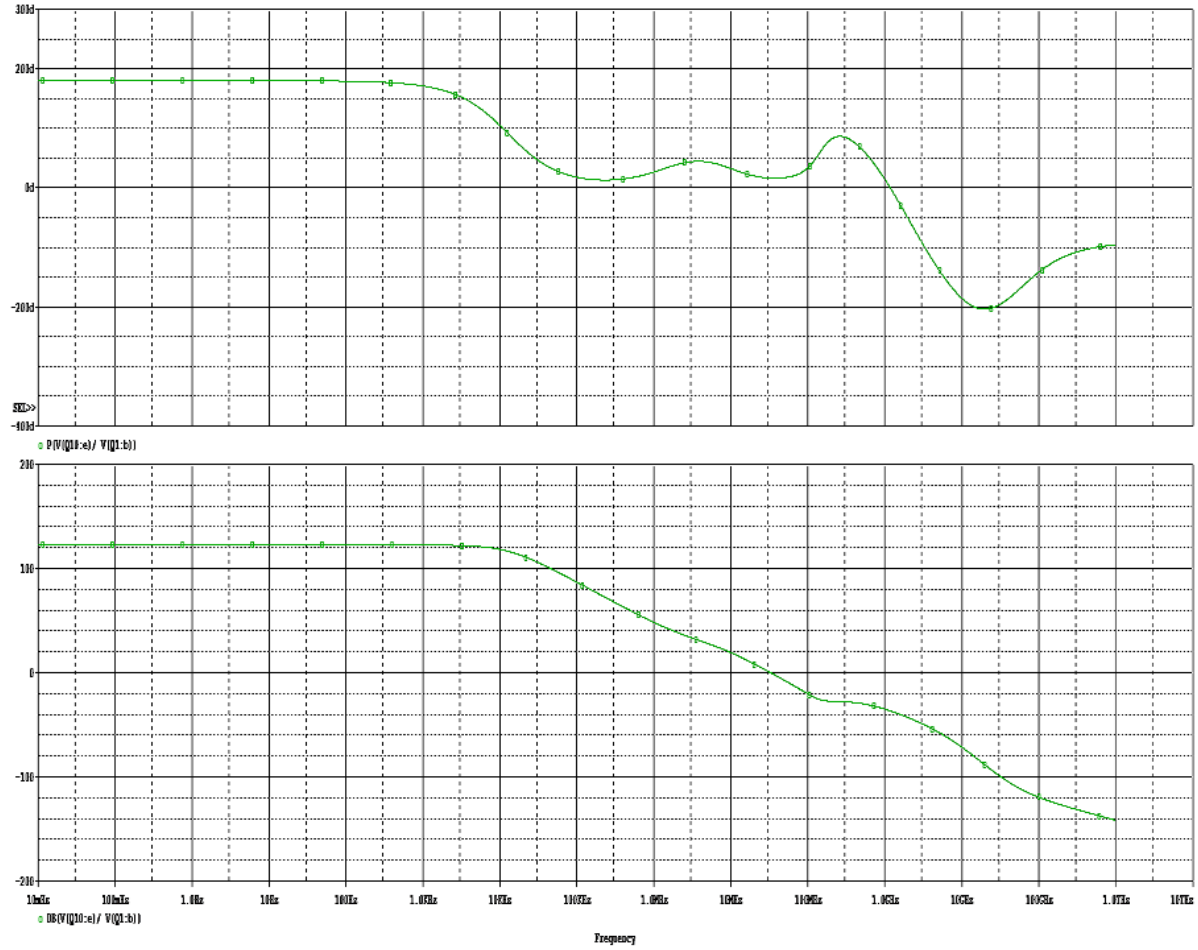

Figure 30: Frequency response without capacitor

DB form expresses gain amplitude based on the equation below.

$$DB = 20 \times log_{10}{}^{gain} \tag{29}$$

Here in this case, the flat part of the gain curve shows that the frequency response is around 122dB in decibel form, or saying 1258925.412 in usual form, within a reasonably low frequency range for this amplifier.

Also, the second method of obtained the bandwidth can be applied using the response 122dB. $f_H = 122dB - 3dB = 119dB$. If we find this response in the gain graph and draw a vertical line across this value we can roughly find that the corresponding f we will obtain is also located in the area under the corner where we drew tangent line in the previous graph.

For the phase plot in the lower graph, it can be seen that the phase also remains unchanged within a reasonably low frequency range which means that during the range where both two plot remain flat, the angle of the gain is not changed and the amplifier has very stable gain with the same amplitude and phase.

3.3.2 Task 2

The simulation graph for the frequency response with a capacitor added is shown in Figure 31.

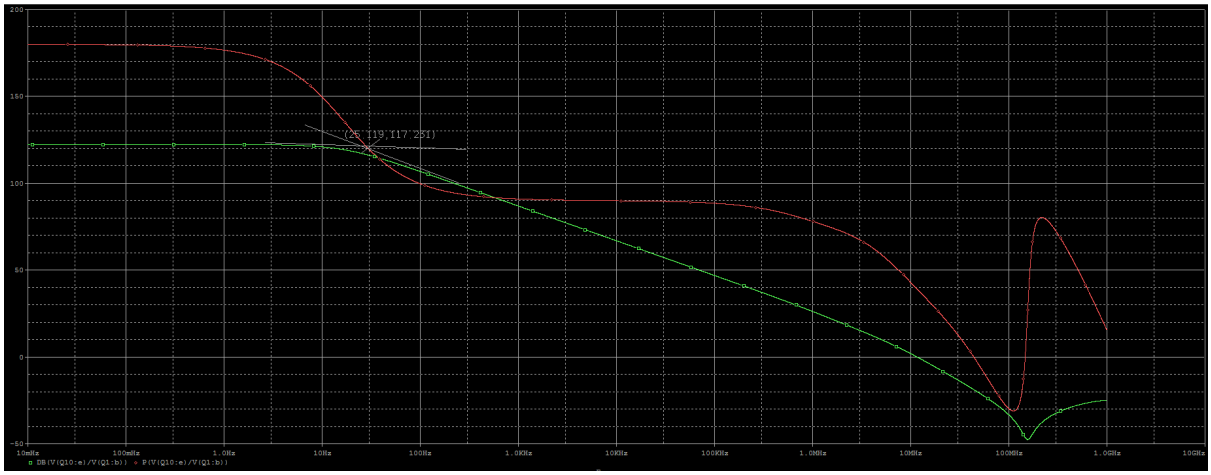

Figure 31: Frequency response with capacitor

Phase margin

Similarly as what we did previously for the case without capacitor added, we can obtain the phase margin, which is around 40 degree.

This indicates that the addition of the compensation capacitor effectively increases the phase margin, which means that it actually increases the stability of the amplifier since the greater the phase margin is the more stable the amplifier will be as learnt from lectures.

Bandwidth

It can be seen that the bandwidth of the amplifier with the compensation capacitor can be seen as approximately $25.119Hz$ based on the same method as discussed for the case without capacitor as can be seen in the intersection points of the two tangent lines.

It is apparent that this value of bandwidth is much smaller that that obtained in the case without capacitor added. This indicates that the addition of that compensation capacitor make a difference on the bandwidth, that is decreasing the bandwidth effectively.

The DB form gain amplitude plot and the phase plot in different graph with the addition of a compensation capacitor can be seen in Figure below.

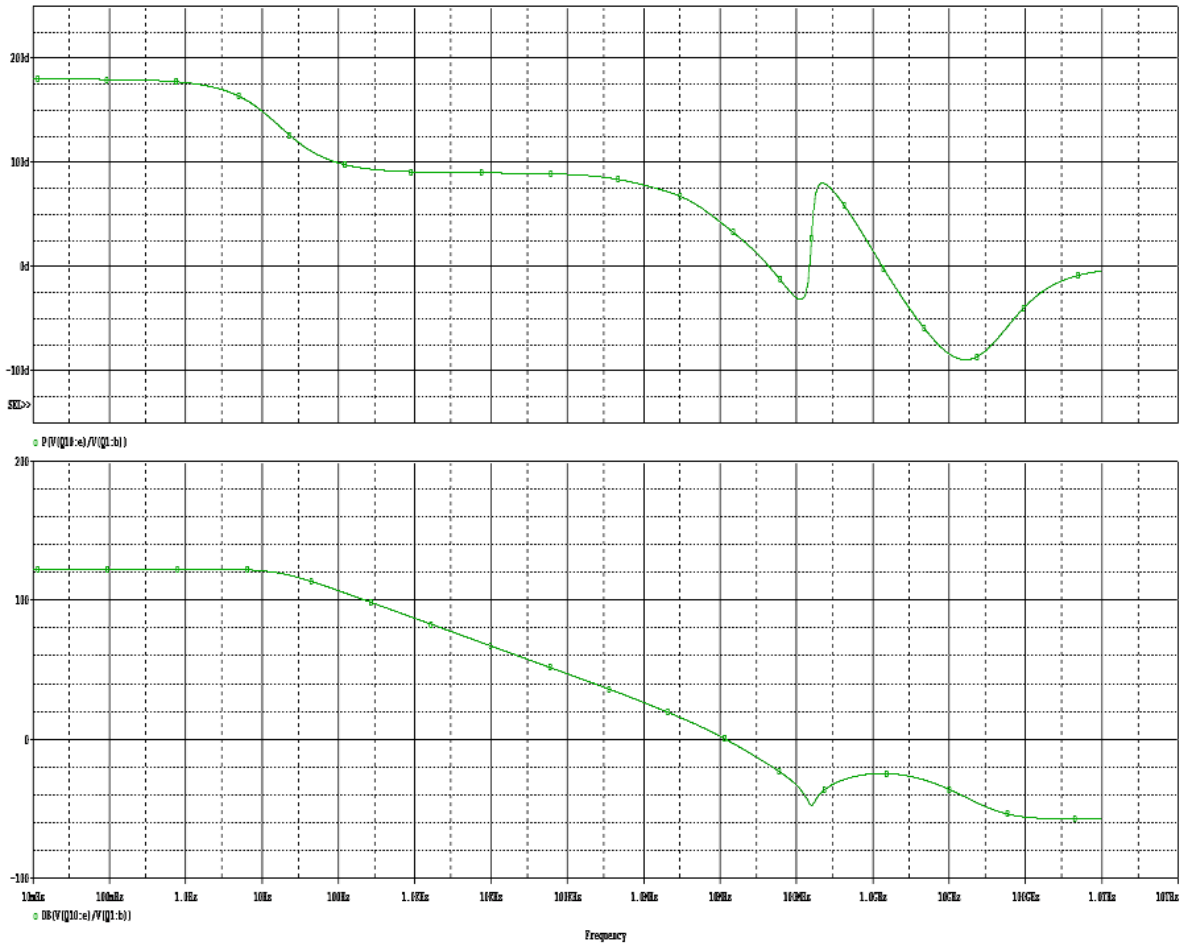

Figure 32: Frequency response without capacitor

Here in this case, after adding the compensation capacitor, the curve slightly changed compared to that obtained without the capacitor mainly on the corner frequency area.

However, the frequency response after adding that capacitor is still around 122dB. This indicates that the compensation capacitor make no effect on the response of the gain amplitude.

For the phase plot in the lower graph, it can be seen that a wider range of frequency where the phase remains stable is appearing in a range around from 100Hz to 1MHz if we look at the axis carefully (This might not be obvious if we still use usual logic of viewing axis since in these task, the log form is applied in the horizontal axis which means the value in lower range is displayed thinly while in higher range the values are displayed much more concentrated).

3.3.3 BONUS

The simulation graph for common-mode source with voltage gain trace added is shown in Figure 33, and that with a compensating capacitor added is shown in Figure 34.

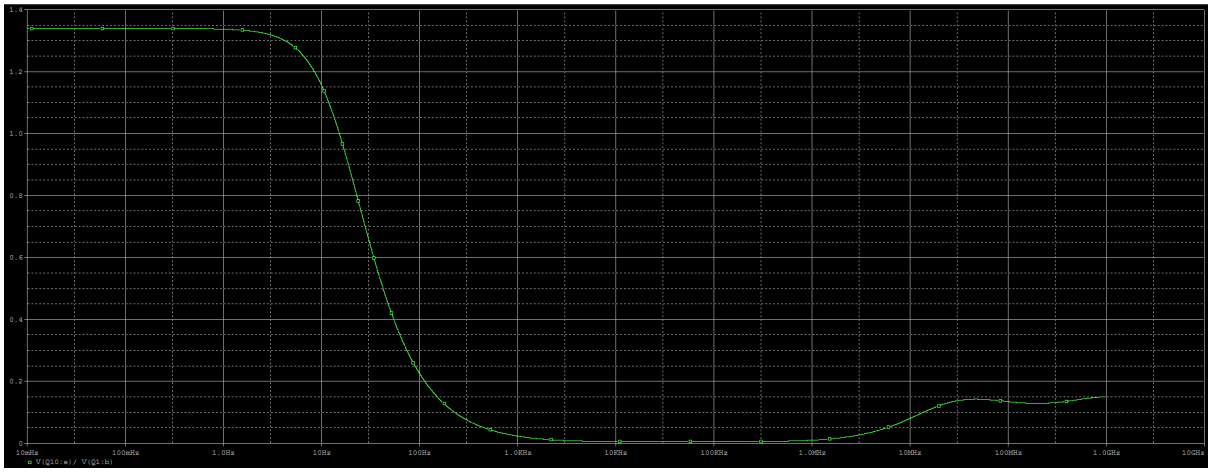

Figure 33: Response for common mode signal

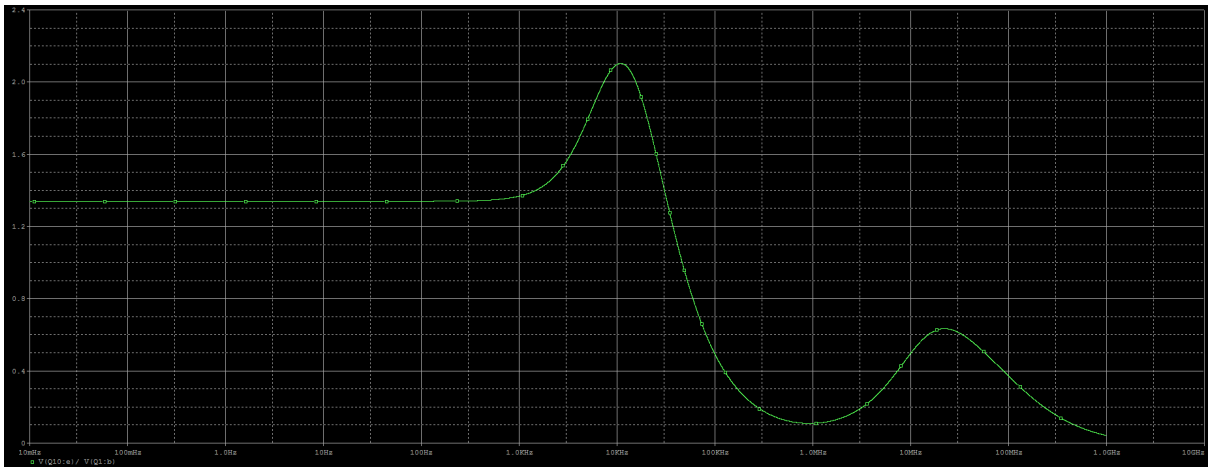

Figure 34: Response for common mode signal with capacitor existing

The voltage gain for common-mode source is simply slightly bigger than 1, which indicates that the common-mode signal indeed cannot be significantly amplified by amplifier. Comparing the two graphs, it can be seen that when a compensation capacitor is added, the flat area of the curve is enlarged which means the stable frequency range is increased by the addition of the capacitor.

4 Discussion

4.1 General Question

- 1. What can be deduced about the amplifier stability from the Bode plots in Part III?
  - Overall, the operating amplifier is designed in an open loop system, and the stability of it can be estimated through phase/gain margin. Gain margin is defined as the difference between 0dB and voltage gain at a 180 degree phase. Phase margin is the difference between 180 degree and the phase shift where voltage gain crosses 0dB [7].
  - To deduct the stability of the amplifier from the Bode plots, we first consider the fact that the operating amplifier (the closed loop circuit) is stable when the phase margin is big enough [7].
  - The method of obtained the phase margin is illustrated in Figure 35, which is to first draw a horizontal line at 0dB for the gain curve (green curve in Part III simulation graphs); then, a vertical line across the intersection point should be draw and the intersection point of this line and the phase curve (red curve) is obtained; and finally, the difference of these two vertical components of the points is the phase margin. This is how we calculated the phase margin in Part III.

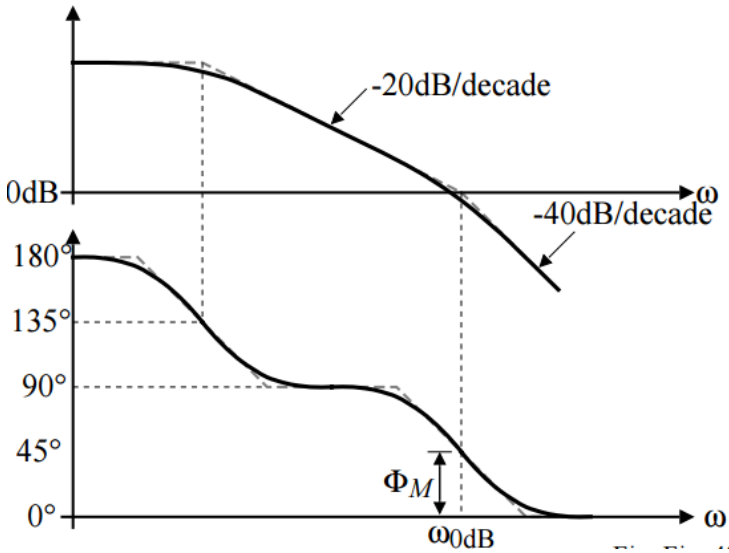

Figure 35: To obtain phase margin

  - As discussed in result section the phase margin with and without capacior are 18 degree and 40 degree respectively, therefore the system with the capacitor added is more stable. However, despite the fact that the larger phase margin is, the more stable the system is, if it is too large, slow time respond speed might be caused, therefore, the suggested range of phase margin is from 45 to 70 degrees [7].
  - In summary, the process of deducing the stability can be: we can first find out the frequency response of the amplifier, with the frequency being in phase in the stable range which is the flat area for the gain curve [8]; then the gain can be found and the gain margin is obtained, which is minus gain; when the corresponding gain value is 0 (as discussed in detail above), the phase value is found. The bigger the phase margin is, the more stable the amplifier is.

- 2. What is the purpose of the "Phase compensating capacitor"?
  - After observing the simulation results from Part III, apparently, the compensation capacitor reduced the bandwidth of the amplifier, increase the phase margin, but did not effect the frequency response when the frequency is not too high.
  - The stability can be effectively increased by adding the capacitor mainly because the phase margin can be increased by the addition of the "Phase compensating capacitor" [8]. Therefore, the purpose of adding this capacitor is to increase the stability of the amplifier.
  - Ideally the gain should be stable for all frequencies but in practice, this is impossible. The gain starts to fall when the frequency is very high. The part where the frequency starts to drop is break-point and the break-point used in this case is the 3dB point. There are many reasons for this break-point and the main reason is the frequency compensation. For gain curve in decibel format, 20log10(gain) is the vertical component for the green curve in simulation graphs in Part III, and the bandwidth of the amplifier we found using two tangent lines is where the gain is reduced by 3dB [5].
  - As has been discussed in result section, it can be deduced that the phase compensating capacitor actually improves the stability of the system. In detail, the compensating capacitor decreases the bandwidth of the amplifier f_H. Because of this limitation of the bandwidth, the frequency of 0dB point become smaller while the phase margin become bigger correspondingly.
  - In summary, almost always the properly designed amplifier should be stable for the entire frequency band and the most common way to do that is by using a compensation capacitor.

4.2 Design Specification

As can be seen in Table 2, all the specifications have been met by this design.

Table 2: Design specification table

Parameter	**Specification**	**Your value**	**Comment**
Differential input impedance	$> 100k$	$140k$	The value used in design was an initial assumption, based on which the calculation was started.
Open loop voltage gain	$> 500,000$	$-1,288,960$	The gain obtained from simulation graph using both two methods as have been discussed in Part II task 3 and 5 were much bigger than the required minimum gain.
Output impedance	$< 1k$	970	Both the initially assumed value and the simulated value are smaller than the maximum restriction.
DC output voltage	$\approx 0V$	$-3.347m$	The simulated value generally meets the requirements since this magnitude is very small thus can be seen as zero.
DC offset voltage	None given	-107.111μ	This was obtained from task 4 in part II
Frequency response	Down to DC (0Hz)	maximum is 122dB	The frequency response, the gain amplitude in decibel form, reduced from 122dB with the increase of frequency after the lower range of frequency where response remains stable ends.
Total current consumption	$< 5mA$	$2.402m$	Simulated value is less than the maximum
Bandwidth with compensation capacitor	None given	25.119	This was obtained from task 2 in part III.

More detailed comments are listed below:

Open-loop gain

The requirement on the open-loop gain value is no less than 500,000. The two gain value obtained in the experiments are 1268825.612 and 1288960 (both has minus mark) respectively.

It is apparent that the designed amplifier has a voltage gain which meets the specification even taken some simulation error into consideration since the obtained value is much bigger than the required minimum value.

DC offset voltage

The value of the DC offset voltage obtained in this experiment is $-107.111\mu V$. There is no specific requirement on the value of it in the specification, so we do not need to make any more comparison for this parameter since itself is a very small value and is existing because of the unideal reality of amplifier rather than an essential factor that directly dominate the amplifier function feature.

Ideally, there is no need for the existence of this DC offset voltage. However, in reality, there is indeed a DC offset between tow inputs of a real amplifier. This value is not a parameter that can be designed exactly at the first stage but should be obtained through actual simulation result after designing all the other essential components such as resistors and configuration.

DC output voltage

In Part II task 7, the DC output voltage can be seen is -3.347mV. This experimental value is actually quite close to the requirement that the output should be zero when input is zero, thus this parameter also satisfy the specification.

This voltage means that when the amplifier dose have any input signal, there is virtually no output signal generated as well since this DC output voltage obtained is very small. However, in real world, this voltage still exists no matter how small it is, this is caused by the existence of the DC offset voltage which is also caused by the device internal situation is not as perfect as expected.

Total current consumption

The total current consumption obtained in this experiment is 2.402mA. This value is apparently smaller than the required maximum value of it that is 5mA. Therefore, this parameter meet the specification as well.

For am amplifier, this value of current consumption is expected to be small enough mainly because no matter in what cases in terms of engineering design, the reality practice should be considered and the power consumption is a very essential real problem worth considering. With low current consumption for the internal circuit of the amplifier, the circuit using it can save power as a result.

Frequency response

The gain value is around 122dB in decibel form, or 1258925.412 in usual form, and even after adding a compensation capacitor to the designed circuit, this value did not change basically.

With the increase of the frequency range, the gain will change with it in a trend expressed as equation below, where $r_{b'e}$ and $r_{bb'}$ are transistor internal resistance.

$$A_V = -g_m \times R_t \times \frac{r_{b'e}}{(r_{b'e+r_b b'+R_S})(1 + j(\frac{f}{f_H}))} \tag{30}$$

As can be seen in equation, when the frequency is much smaller than the f_H, the phase difference can be regarded as 180 degree and the voltage gain obtains its maximum value. This is why in Part III, the response graphs for gain amplitude have flat region in the low frequency range before the frequency increases to f_H.

Bandwidth with compensation

The bandwidth value with the compensation capacitor added obtained in this experiment is 25.119Hz. This value is much smaller than that obtained when there was no capacitor added. The reason for this can be explained using Miller's Effect small signal diagram transform.

Bandwidth of an amplifier is also called the corner frequency. This frequency can be obtained from the simulation value using two methods as have been used respectively in Part III result section. One is to draw two tangent lines at the "corner" regain on the amplitude curve where roughly the corner frequency should lie in, and then draw a vertical line through the intersection of two lines and find the corresponding frequency in the axis. the other method is to use the feature that gain reduces 3dB at corner frequency.

4.3 Error Analysis

The assumed value and simulated value of R_{OUT}
Error: The assumed value which was used in the calculation process was 800Ω, while the simulated value obtained from the task 6 in part II was around 970Ω which although still met the specification that output impedance should be no bigger than $1k\Omega$, was bigger than the assumed value.
Analysis: This difference between the theoretical value and the experimental value might has been caused by the approximation we adopted during the calculation process such as the ignorance of the base currents, which apparently would not be ignored by the simulation tool.

The calculated value of gain using methods from task 3 and 5 in part II
Error: The calculated gain value was -1268825.612 and -1288960 respectively, which are slightly different from each other, although they still both met the specification that the gain should be no less than 500,000.
Analysis: This might have been caused by the step number set for the simulation. For example, the more number of steps chosen for one simulation, the closer the simulated value would be to the so-called most accurate value. However, the mode chosen for the simulation were already difference for these two method, the amplitude set for the source was different as well, the step number choice might have different extent of influence on the accuracy of the simulation.

The calculated value of the four resistances
Error: The resistances calculated themselves might not be completely accurate due to approximations as discussed and some other parameter values usage such as β. Also, even we assume that the tiny error that might be caused by factors as mentioned above, in real implementation, these values might not be all achieved practically.
Analysis: This is because the available resistors in lab tend to be standard resistors with a set of certain value which apparently do not cover all the real number. However, the calculated resistances were all very concrete number with several numbers after the decimal point, which are impossible to be found from standard resistors. Also, even there are adjustable resistors available, it would be impossible to accurately adjust to the expected value.

4.4 Suggestions

Make less approximation in calculation
Some of the approximations can be changed into more accurate calculation step. For example, the base voltage of each transistor that are involved in the calculation process can be also worked out and considered.

Apply more steps when simulating
To make the simulation more accurate, more steps can be set for each simulation. However, this might require higher quality of the computer in which the simulation software run, therefore, more powerful computers with lots of memory is suggested to be used.

Obtain more accurate value for β
The β used in this design was the value obtained using the method provided by part I which was to get the current gain for AC mode approximately based on the reading of DC sweep of transistor characteristics curve. This method can be optimized further by adopting smaller space for each two steps of the I_B sets thus more sets of I_B and I_C pairs can be obtained and the calculation would be more reliable.

5 Conclusions

5.1 Objective achievement

The objectives of this design assignment were successfully met since the virtual amplifier designed indeed fitted all the specifications which were from limitations on the total value of the current consumption, output impedance to the minimum gain magnitude.
Also, the existing errors (though did not influence the success of the design according to the specification) were analyzed and reflected, and some corresponding suggestions on solving them were proposed.

5.2 Limitation and suggestion

Despite of the general success of the design, there are still some limitations existing in this design. For example, the resistances value calculated and used in the design would not be completely adopted in the practical implementation of the amplifier since there are only a limited number of values for standard resistors.This can be solved by adopting standard resistor values in the design after obtaining the calculated resistances and adopt simulation to test and further adjust the resistance.

5.3 Further improvement

For calculation, more powerful mathematical process can be adopted to avoid trails and errors using the calculation function–Transcendental equations are suggested so that the equations can be generated based on some inequality relationships based in the specification and the results can be certain range of the value rather than only one particular set of values tried out.
For research extension, the components composition in the design can be made more scientific such as adding a resistor in series with the compensation capacitor to achieve more scientific miller connection.

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[8] P. Bibby, "lecture notes part seven," http://www.psychology.nottingham.ac.uk/staff/dmr/c81mpr/HOWTOWRITEALABORATORYREPORT.pdf, University of Nottingham, Sep. 2006.

Appendices

A Program Listings

The function used to calculate the four resistances is listed below.

Listing 1: This is how to include some source code

```
function [R1,R2,R3,R4] = calculation(V_R2,V_OUT)



R_id=110000;
%The differential input impedance is assumed to be slightly bigger than 100k



V_CC=9;
V_EE=-9;
V_BE=0.6;
V_T=0.025;
V_Anpn=72;
V_Apnp=116;
beta_npn=179;
beta_pnp=232;
%Parameters whose values have been already known



I_C5=beta_pnp/10/R_id;

R2=V_R2/I_C5;
%R2 can be first worked out after obtaining I_C5



I_C6=I_C5*exp(R2*I_C5/V_T);

R1=(V_CC-V_EE-V_BE)/I_C6;
%R1 is the second resistance that can be worked out once R1 is worked out



rce2=V_Apnp/(I_C5/2);

rce4=V_Anpn/(I_C5/2);

rbe9=beta_npn/(I_C6*40);

rce8=V_Apnp/I_C6;

rce9=V_Anpn/I_C6;
%Some impedance values that will be used to obtain R3 and R4




```

```
A=rce2*rce4/(rce2+rce4);          %rce||rce4
B=beta_npn+1;
C=rce8*rce9/(rce8+rce9);          %rce8||rce9
%To express the complex equation more easily, middle parameters are introduced

R4= -(beta_npn*rbe9 - (160000*A^2*V_BE^2 - 32000*A*B*V_BE^2*rbe9
+ 800*A*V_BE*beta_npn*rbe9 + 1600*B^2*V_BE^2*rbe9^2 + 80*B*V_BE*beta_npn*rbe9^2
+ beta_npn^2*rbe9^2)^(1/2) - 400*A*V_BE + 40*B*V_BE*rbe9)/(2*beta_npn)
%The equation with only one unknown parameter R4 is obtained from the "solve"
%function listed in the end


R3=  (V_OUT*beta_npn - 360*C + 360*(B^2*V_OUT^2 - 2*B*C*V_OUT
+ (B*V_OUT^2*beta_npn)/180 + C^2 + (C*V_OUT*beta_npn)/180
+ (V_OUT^2*beta_npn^2)/129600)^(1/2) + 360*B*V_OUT)/(2*beta_npn);
%The equation with only one unknown parameter R3 is obtained from the "solve"
%function listed in the end



rce2
rce4
rce8
rce9
%display these important middle parameters used during the calculation as well


%*********the equation used to generated the expressions for R3 and R4***********

%R4=solve('beta_npn*R4/(40*V_BE)+B*(R4*rbe9/(R4+rbe9))=10*A','R4');

%R3=solve('((C+beta_npn*R3/(40*9))/B)*R3/(R3+((C+beta_npn*R3/(40*9))/B))=V_OUT','R3');




end
```