UNIVERSITY OF LIVERPOOL

# Experiment 5 - Design of an Operational Amplifier Using PSpice

ELEC271*

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**Abstract**

In this report, an op-amp meet all of the specifications was designed and simulated to measure a set of parameters. This op-amp has a differential input impedance of 141kΩ and a output impedance of 852Ω. This op-amp needs a 9V $V_{CC}$ and -9V $V_{EE}$ DC supply and has an open-loop voltage gain of 1,287,968. The total current consumption of this op-amp is 2.316mA and the frequency bandwidth is 7.7kHz. In this experiment, PSpice was utilized to design the schematic and simulation.


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# Contents

# 1 Introduction

## 1.1 Background

Operational amplifier (op-amp) is one of the most broadly utilized electronic components when designing sound equipment, signal processors, RF circuits etc. Due to its characteristics that the gain can be independently decided by the external design with negative feedback [1], op-amp can achieve precise and customized functions with competitive cost. Besides, as it shown in Figure 1, op-amp can also accept both signal-end and differential input while the latter feature could considerably benefit the RF amplifier circuit (LNA) design [2].

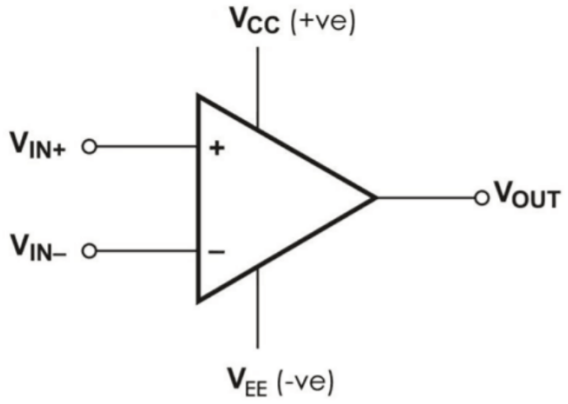


Figure 1: Op-amp Symbol with Differential Input (taken from [1])

In addition to the differential input, op-amp provide a signal end output containing differential part of original signal. As it shown in Figure 1, op-amp is a typical active component and is required to be powered with $V_{CC}$ and $V_{EE}$.

## 1.2 Objectives

The objective of this experiment was to design a op-amp consists of four building blocks including emitter followers, common emitter amplifiers, current mirror circuits as well as a differential input stage. To be specific, with PSpice software, models of Q2N2222 NPN transistor and Q2N2907 PNP transistor could be utilized. Design specifications is shown in Table 1.

Table 1: Op-amp Design Specifications

| Item | Requirement |
|---|---|
| Differential Input Impedance | $\geq 100k\Omega$ |
| Voltage Gain | $\geq 500,000$ |
| Output Impedance | $\leq 1k\Omega$ |
| Output Voltage | Be zero for zero input |
| Frequency Response | Down to DC |
| Supply Voltage | +9 to -9 volts |
| Total Current Consumption | $\leq 5mA$ |

### 1.3 Theory

A typical op-amp consists of 5 parts as it shown in Figure 2. Part 1 and the upper part of part 2 consists of a mirror circuit to provide a stable and precise DC input $I_2$ for the differential amplifier Q3 and Q4 in part 2. In part 2, it can be noticed that the two transistors Q5 and Q6 also consist a mirror circuit which ensures the circuit go through Q3 and Q4 are equal while transistors Q3 and Q4 function to accept and amplify the input differential signal. Part 3 and part 5 are emitter followers which aims to decrease the output impedance without changing the amplitude of the signal. Transistor Q8 in part 4 is a typical CE amplifier while Q9 with the circuit in part 1 makes up a mirror circuit to provide stable current for Q8.

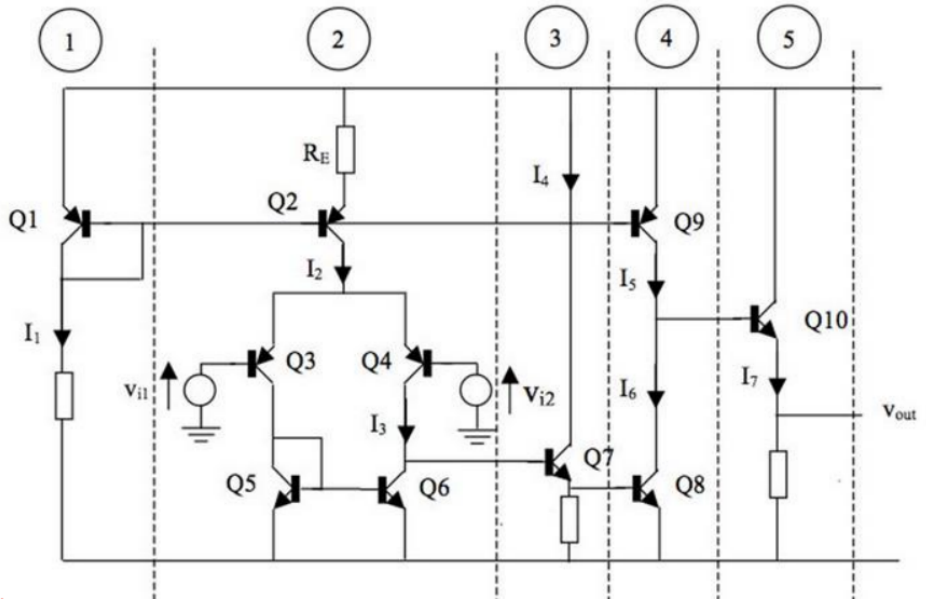


Figure 2: Op-amp Inner Circuit Perspective with Part Number (taken from [3])

In above Figure 2, the differential signal was firstly input from $v_{i1}$ and $v_{i2}$ and then the differential part of the signal is amplified and transmitted from the line above Q6 to Q7 in part 3. In part 3, the output impedance of the signal was significantly decreased while the gain of the signal remains. When it comes to part 4, it is amplified again to get a higher gain. Then in part 5, the output impedance of the signal is decreased again to be prepared for the output at *Vout*.

The challenge of this design work is to calculate the value of the 4 resistors to meet the design specifications given. Besides, designing necessary and effective surrounding circuit for simulating the parameters such as gain, input and output impedance, and frequency response is also required.

# 2 Materials and Methods

## 2.1 Calculation

### 2.1.1 Known Parameters

Table 2 shows the value of known parameters. There parameters will be utilized in the following calculation.

Table 2: Op-amp Design Known Parameters

| Parameter | Value |
|---|---|
| $V_{CC}$ | 9V |
| $V_{EE}$ | -9V |
| $V_{BE}$ | 0.6V |
| $V_T$ | 25mV |
| $V_{A(npn)}$ | 72V |
| $V_{A(pnp)}$ | 116V |
| $\beta_{npn}$ | 179 |
| $\beta_{pnp}$ | 232 |

As it shown in Table 2, the supplied voltage $V_{CC}$ and $V_{EE}$ are expected to be 9V and -9V. The voltage of PN junction of $V_{BE}$ is supposed to be 0.6V and the early voltage of npn and pnp transistors are desired to be 72V and 116V while the value of $V_T$ is 25mV. The gain of transistors Q2N2222 and Q2N2907 are simulated to be 179 and 232 which could be found in the following result section.

### 2.1.2 Assumption

Table 3: Op-amp Assumption

| Parameter | Value |
|---|---|
| $R_{id}$ | $140K\Omega$ |
| $R_{out}$ | $800\Omega$ |

According to Table 1 the differential input impedance should be no less than $100k\Omega$ and the output impedance should be less than $1k\Omega$. To begin calculation with required specifications, the value of input and output of op-amp were designed to be $140K\Omega$ and $800\Omega$ as it shown in Table 3;

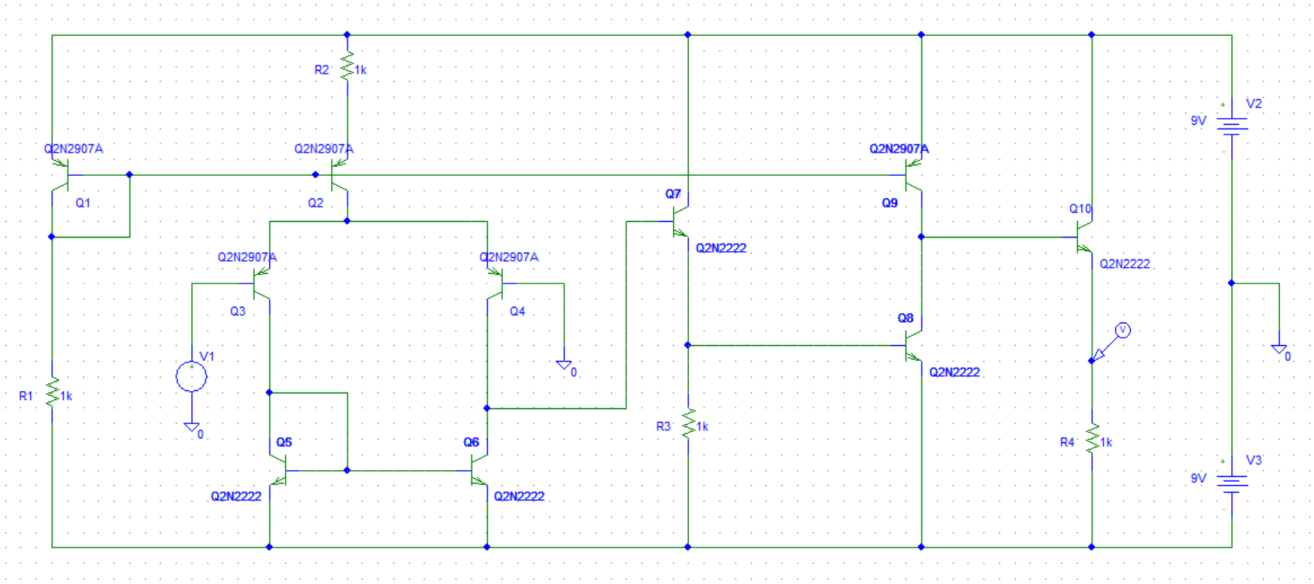


Figure 3: Op-amp Circuit Design

Figure 3 presents another op-amp schematic in PSpice with all the resistors of default $10k\Omega$. This figure will be used to demonstrate the following calculations.

### 2.1.3 $R_1$ Calculation

According to Table 1, the total current consumption should be less than 5mA. Therefore, it is reasonable to assume that the current of each part should be less than 1mA since there are five parts. Thus the value of $I_{R1}$ could be suggested to be 1mA.

As the current on wire connecting the base of Q1 and Q2 is much smaller than $I_{R1}$, it could be ignored when calculating the value of $R_1$.

Apply KVL to part1, the following Equation 1 can be obtained.

$$V_{CC} - V_{BE} - I_{R1}R_1 - V_{EE} = 0 \tag{1}$$

Then the value of $R_1$ could be calculated.

$$R_1 = \frac{V_{CC} - V_{BE} - V_{EE}}{I_{R1}} = \frac{9 - 0.6 - (-9)}{1} = 17.4k\Omega \tag{2}$$

### 2.1.4 $R_2$ Calculation

To calculate $R_2$, the assumed differential input impedance $R_{id}$ could be utilized according to Equation 3.

$$R_{id} = 2r_{be} = \frac{2\beta_{pnp}}{40I_{C3}} \tag{3}$$

Because of the mirror circuit consists of transistor Q5 and Q6, the current go through Q3 and Q4 should always be the same. From this, the following Equation 4 can be inferred.

$$I_{C3} = I_{C4} = \frac{I_{R2}}{2} \tag{4}$$

$$I_{R2}R_2 = V_T \ln \frac{I_{R1}}{I_{R2}} \tag{5}$$

With the property of mirror circuit shown as Equation 5 and the above equation, the value of $R_2$ can be calculated as Equation 6.

$$R_2 = \frac{V_T}{I_{R2}} \ln \frac{I_{R1}}{I_{R2}} = 184.48\Omega \approx 180\Omega \tag{6}$$

### 2.1.5 $R_3$ Calculation

In output impedance from the differential amplifier in part 2 can be expressed as following Equation 7.

$$R_{DAo} = \frac{\frac{V_{A(npn)}}{I_{C4}} \times \frac{V_{A(pnp)}}{I_{C4}}}{\frac{V_{A(npn)}}{I_{C4}} + \frac{V_{A(pnp)}}{I_{C4}}} \tag{7}$$

According to the lab script [1], the $R_{in}^{EF}$ approach $10R_{out}^{DA}$.

$$R_{in(CC)} = 10R_{DAo} \tag{8}$$

For the part 3 CC stage, a relationship can be expressed as the following Equation 9.

$$R_{in(CC)} = r_{be7} + (1 + \beta_{npn})R_3||R_L \tag{9}$$

By applying KVL to loop R3-Q8, the following Equation 10 can be obtained.

$$V_{BE} = I_{R3} \times R_3 \tag{10}$$

The value of $r_{be7}$ can then be presented with Equation 11.

$$r_{be7} = \frac{\beta_{npn}}{40I_{R3}} = \frac{\beta_{npn}R_3}{40V_{BE}} \tag{11}$$

Similarly, the value of $R_L$ can be inferred. In part 4, the current value is the same as the current in part 1 because of the mirror circuit.

$$R_L = R_{be8} = \frac{\beta_{npn}}{40I_{R1}} \tag{12}$$

On the basis of the above equations, the value of $R_3$ can then be obtained.

$$R_3 = 462.4k\Omega \approx 460k\Omega \tag{13}$$

### 2.1.6 $R_4$ Calculation

Similar to the method of calculating $R_3$, the value of $R_4$ could be calculated from the assumed output impedance.

$$R_o = (\frac{r_{be10} + R_S}{\beta_{npn}})||R_4 \tag{14}$$

As the structure of part 4 is similar to the right structure of part 2, the output impedance of part 4 (input impedance of part 5) could be expressed as the following Equation 15.

$$R_S = r_{be8}||r_{be9} = \frac{\frac{V_{A(npn)}}{I_{R1}} \times \frac{V_{A(pnp)}}{I_{R1}}}{\frac{V_{A(npn)}}{I_{R1}} + \frac{V_{A(pnp)}}{I_{R1}}} \tag{15}$$

The value of $R_4$ can then be calculated.

$$R_4 = 205.21k\Omega \approx 200k\Omega \tag{16}$$

## 2.2 Part I: Transistor Output Characteristics

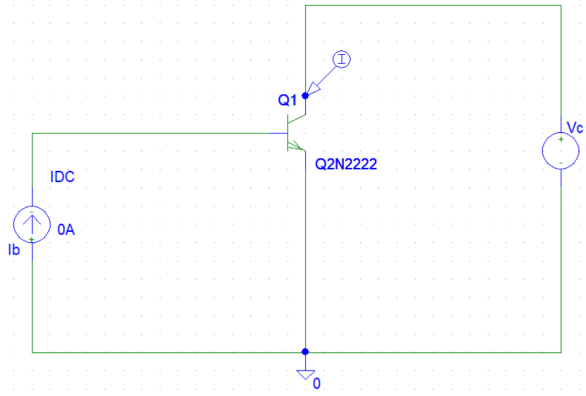


Figure 4: Schematic of Q2N2222

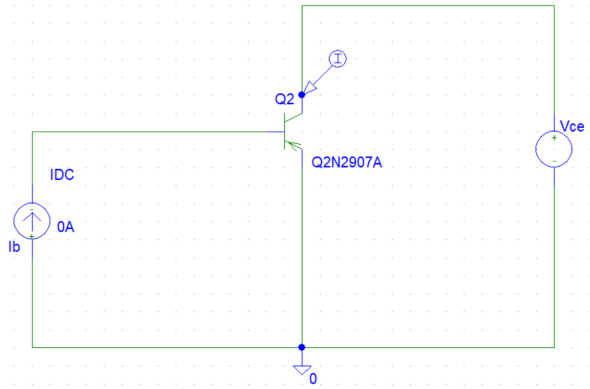


Figure 5: Schematic of Q2N2907

In this part, PSpice was utilized to explore the characteristics of transistor Q2N2222 and Q2N2907. Following the instruction of the supporting materials and the lab script, the test circuits were built as it shown in the above Figure 4 and Figure 5.

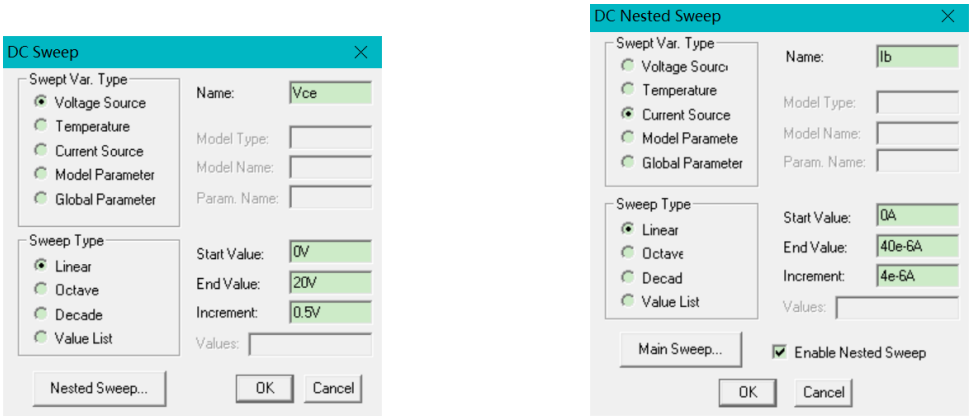


Figure 6: Simulation Setting Windows for Q2N2222

The simulation function of PSpice was used to get a DC sweep with $V_{CE}$ from 0 to 20V and $I_B$ from 0 to 40 uA for npn transistor. On the opposite, for the pnp transistor, the setting of $V_{CE}$ was determined to sweep from 0 to -20V while the $I_B$ sweep from 0 to -40uA. With these setting, the simulation result could be ploted and the gain could be calculated in the result section.

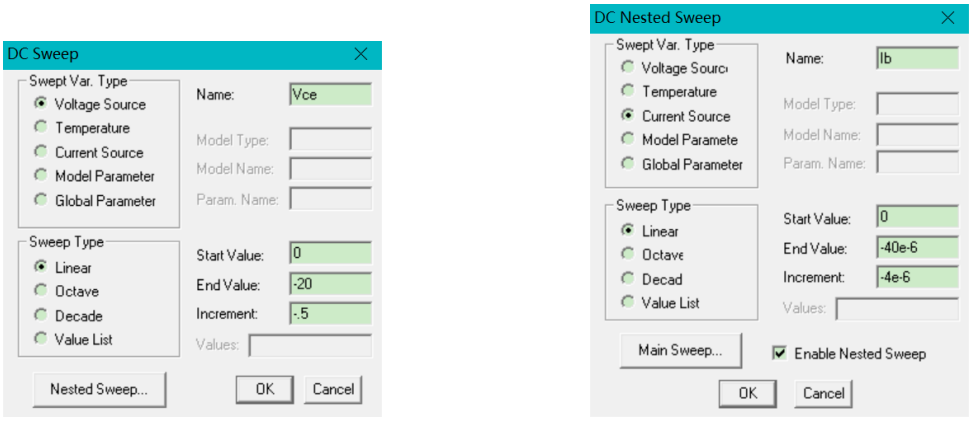


Figure 7: Simulation Setting Windows for Q2N2907

## 2.3 Part II: Achieving the Specification of the Operational Amplifier

### 2.3.1 Task 1

Figure 8 shows the op-amp circuit with a VSCR source to differential amplifier Q3 and GND to the differential amplifier Q4, while the overall circuit is powered with 9V $V_{CC}$ and -9V $V_{EE}$.

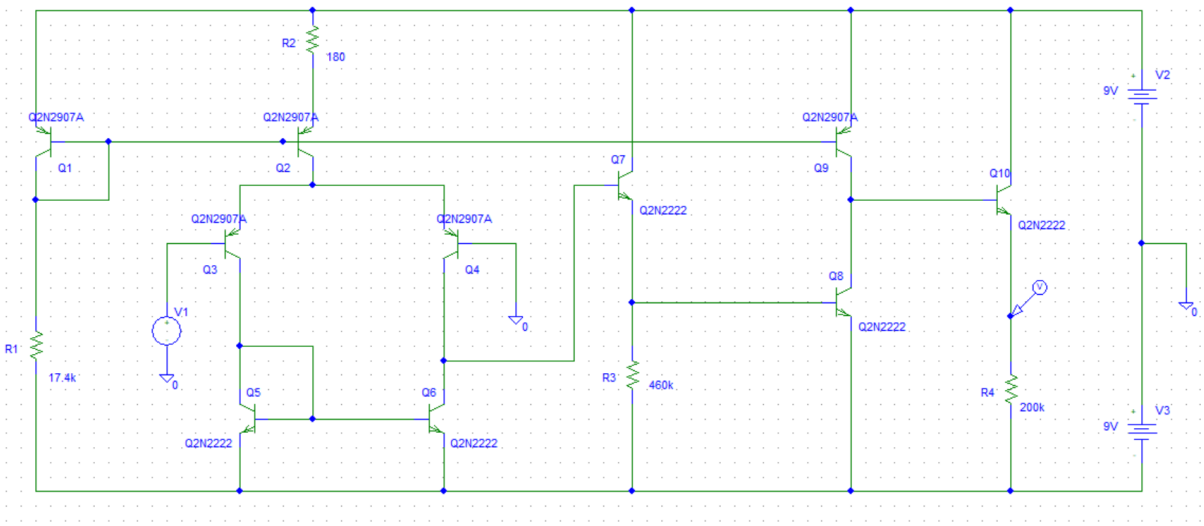


Figure 8: Op-amp Circuit Design with Single-End Input

The four resisters of $R_1$, $R_2$, $R_3$ and $R_4$ are setting to 17.4$k\Omega$, 180$\Omega$, 460$k\Omega$ and 200$k\Omega$ respectively. The calculation details could be found in the above calculation section.

### 2.3.2 Task 2, 3

To find the transfer characteristics and the useful operating range of the op-amp, DC sweep from -9V to 9V with increment of 0.01V was used to identify the dropping part as it shown in Figure 9.

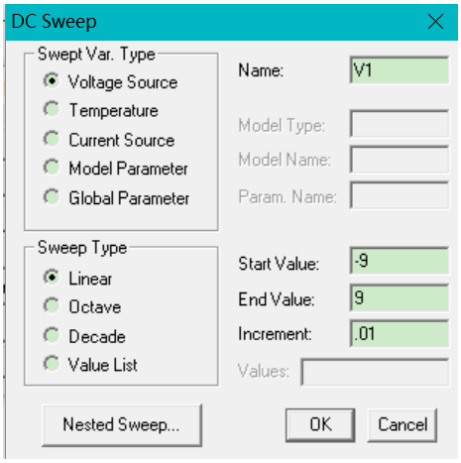


Figure 9: Simulation Setup for DC Sweep from -9V to 9V

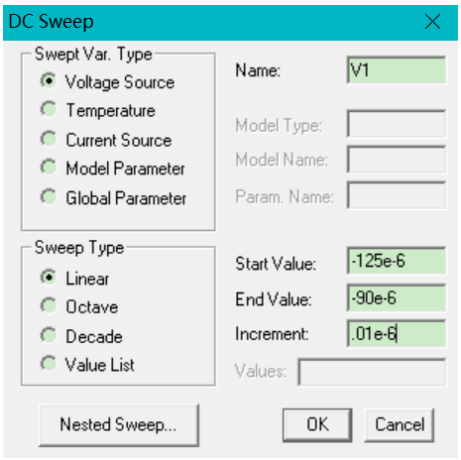


Figure 10: Simulation Setup for DC Sweep from -125uF to -90uV

To further identify the accurate range, opeen loop gain and DC offset, a narrow sweep from -125uV to -90uV with increment of 0.01uV was set as it shown in Figure 10.

### 2.3.3 Task 5

To measure the gain of op-amp, a VSIN was used to substitute the original DC input. New Circuit could be found in Figure 11.

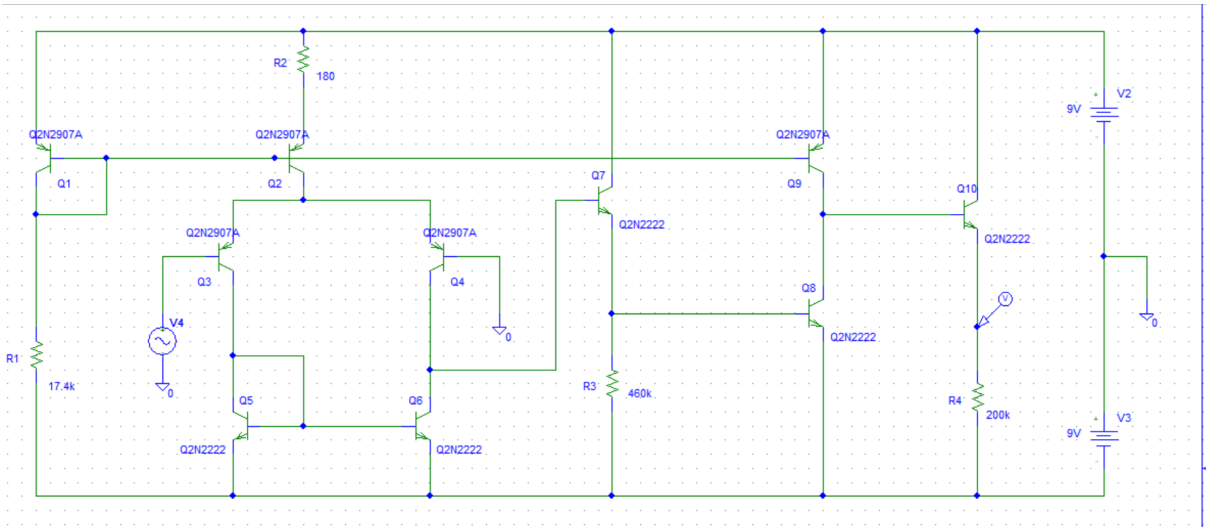


Figure 11: Op-amp Testing Circuit with VSIN

As it shown in Figure 12 and 13, a VSIN was set to be 5uV amplitude with a -108.2uV offset. Then a transient simulation was setup within 4s.

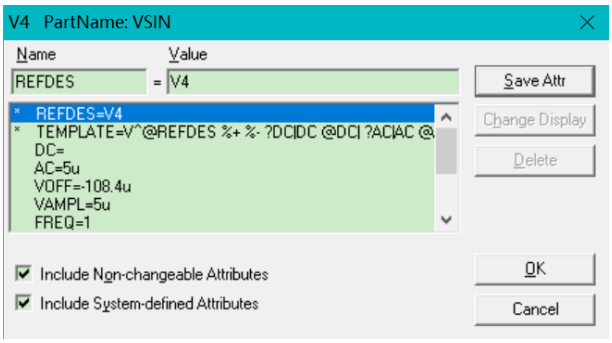


Figure 12: VSIN Setting

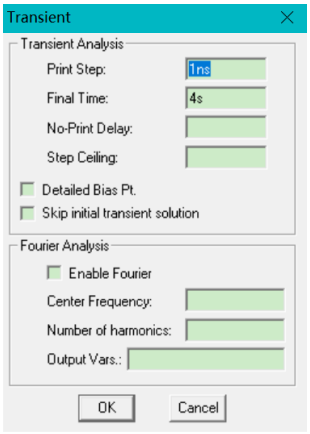


Figure 13: Simulation Setup for Transient from 0 to 4s

### 2.3.4 Task 6

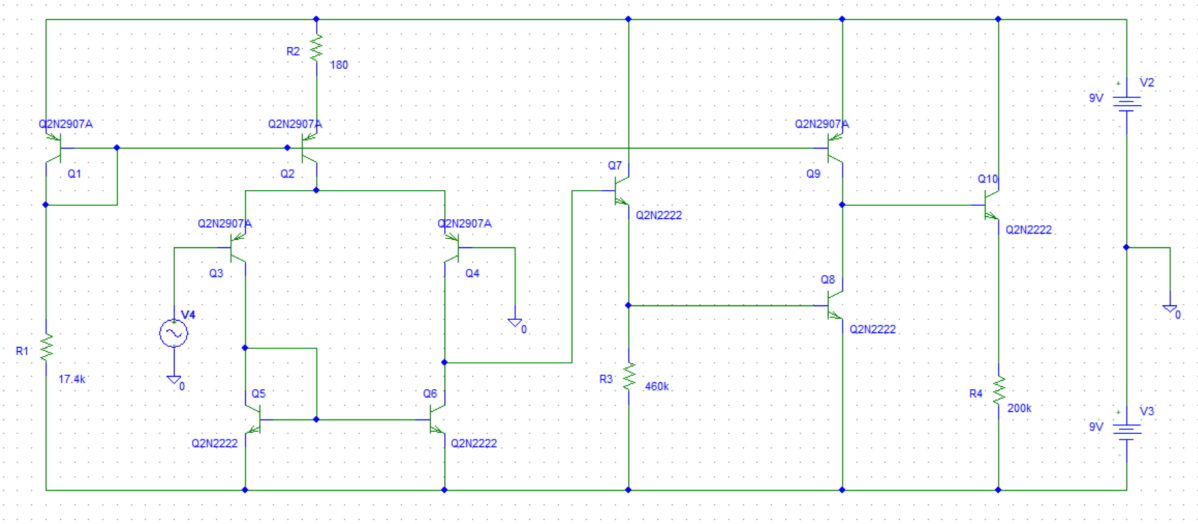


Figure 14: Op-amp Testing Circuit for Input Impedance

Basing on the circuit in Figure 14, a new AC Sweep simulation was conducted to measure the input impedance for different frequency. The input impedance could be represented with $\frac{V_{Q3b}}{I_{Q3b}}$. With the setting of Figure 15.

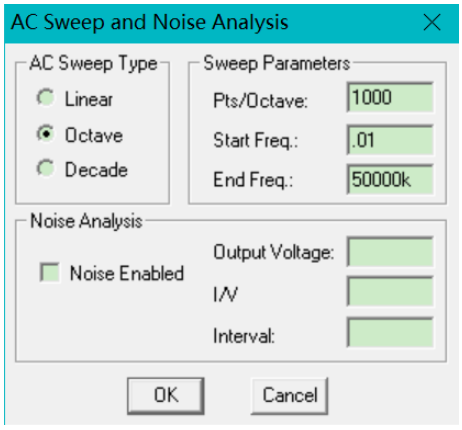


Figure 15: AC Sweep Setting for Testing Input Impedance

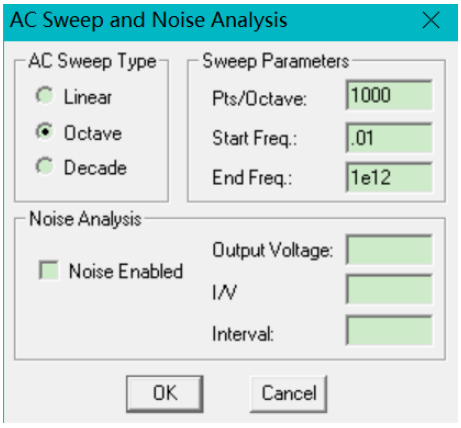


Figure 16: AC Sweep Setting for Testing Output Impedance

To measure the output impedance, the former input port was connected to a -108.4uV DC supply to balance the bias while the output port was connected to a 5uV amplitude VSIN. The relevant circuit can be found in Figure 17.

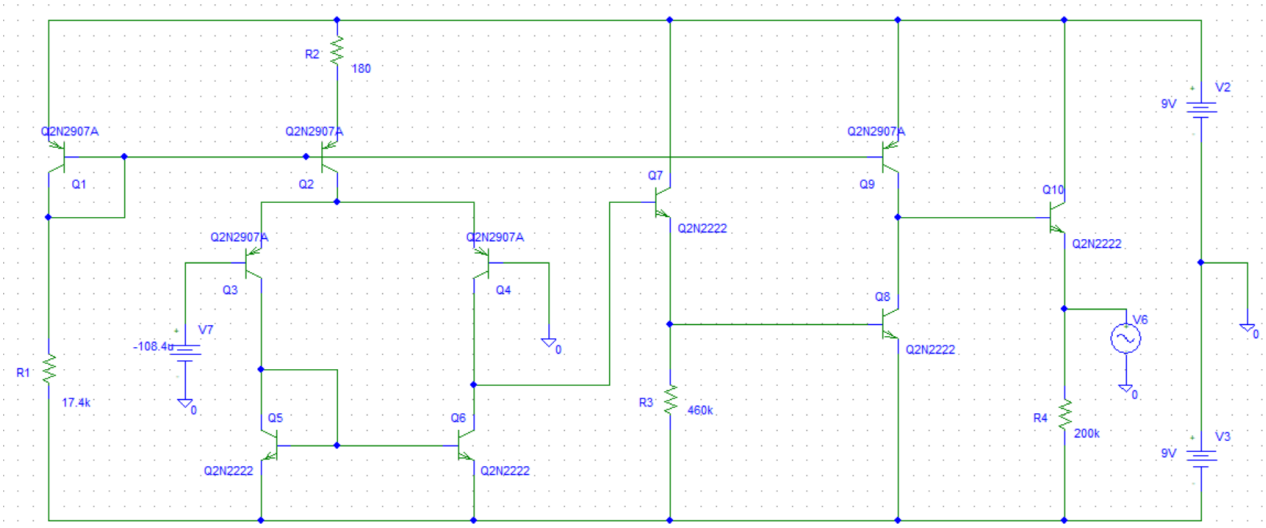


Figure 17: Op-amp Testing Circuit for Output Impedance

After building the circuit in Figure 17, the next step is to set up the AC sweep setting. The corresponding settings can be found in Figure 16.

## 2.4 Part III: Obtaining the Frequency Response of the Designed Amplifier

### 2.4.1 Task 1

Figure 18 displays the circuit that the former VSIN module at input port was changed to VAC for simulation purpose. The Setting of the VAC can be observed in following 19.

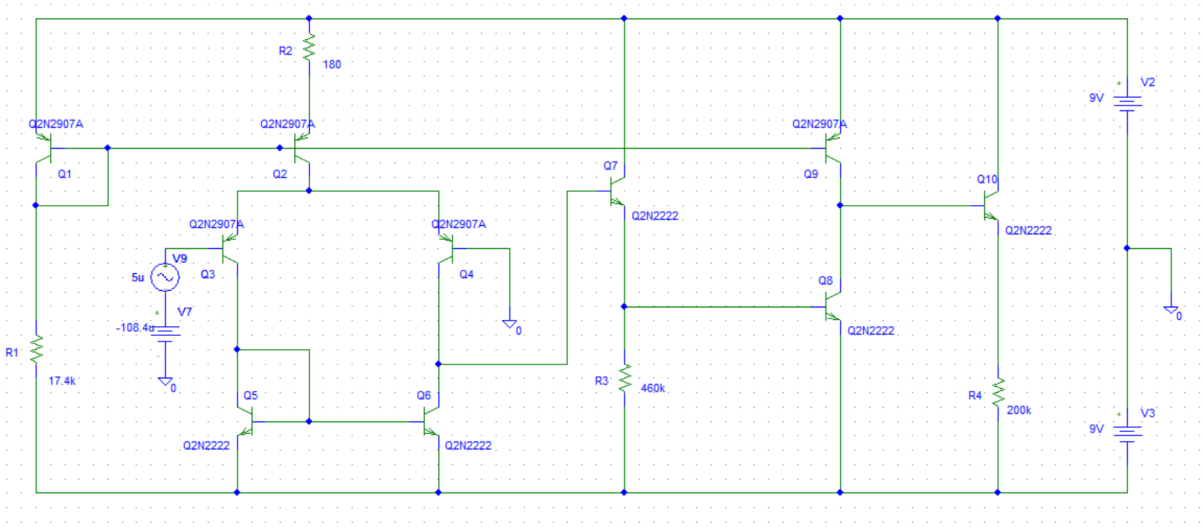


Figure 18: Op-amp Testing Circuit with VAC

Figure 20 shows the setting detail of the AC sweep simulation. In the simulation section, the functions of DB and P were utilized to calculated the result of Bode plots.

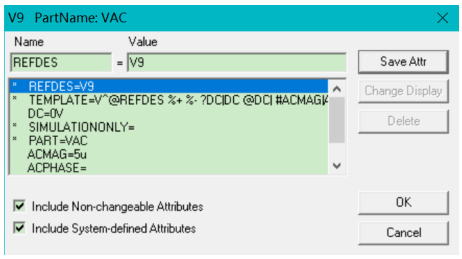


Figure 19: VAC Setting in Figure 18

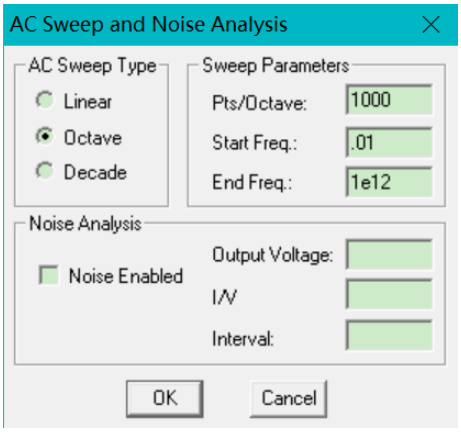


Figure 20: AC Sweep Setting for Getting Bode Plots

Two traces of $DB(V_{e10}/V_{b3})$ and $P(V_{e10}/V_{b3})$ were investigated in the result section.

### 2.4.2 Task 2

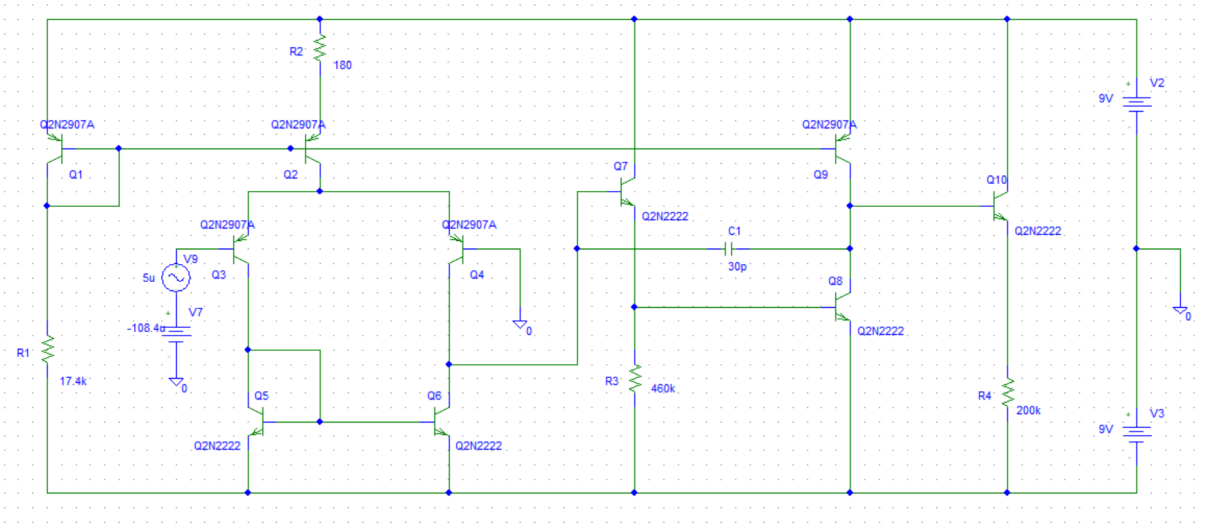


Figure 21: Op-amp Testing Circuit with VAC and Phase Compensating Capacitor

Figure 21 shows the circuit with an additional phase compensating capacitor of 30pF between Q7 base and Q8 emitter. The simulation setting is the same as the last task. Simulation result will be analyzed in the result section.

## 2.5 Bonus Part: Response to Common-Mode Signal

Figure 22 presents the schematic for testing common-mode signal transfer characteristics. It can be noticed that besides Q3 base, the base of Q4, the another differential transistor, was also connected to a AC signal source.

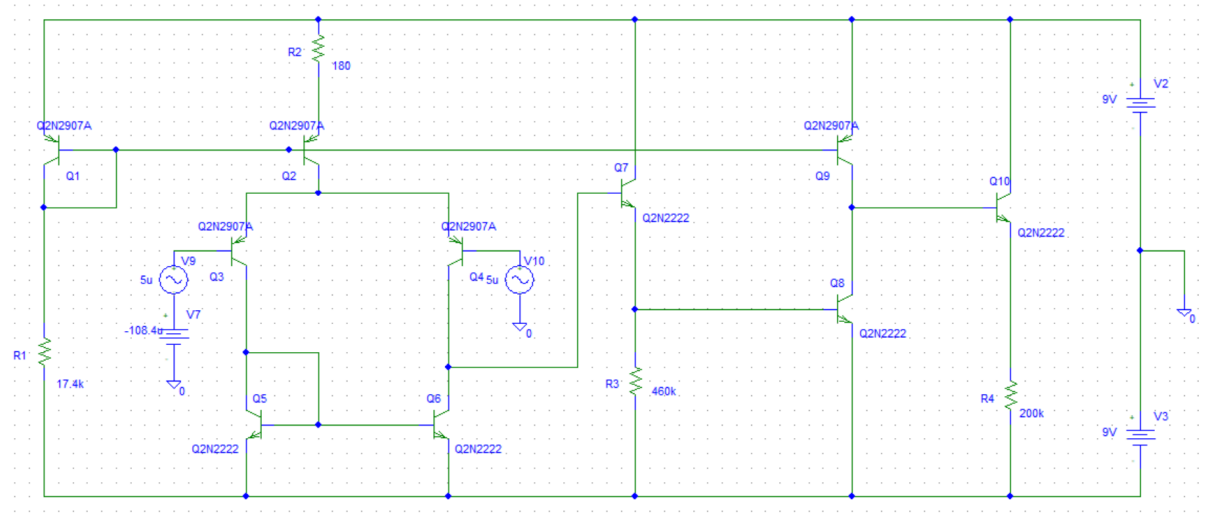


Figure 22: Schematic of Common-Mode Signal Measurement

In the simulation, the trace of $V_{e10}/V_{b3}$ and its average was plotted to investigate the common-mode amplifying property against frequency.

# 3 Results

## 3.1 Part I: Transistor Output Characteristics

The AC current gain of both NPN and PNP transistor can be obtained with the following equation 17.

$$\beta_o = \frac{\Delta I_C}{\Delta I_B} \tag{17}$$

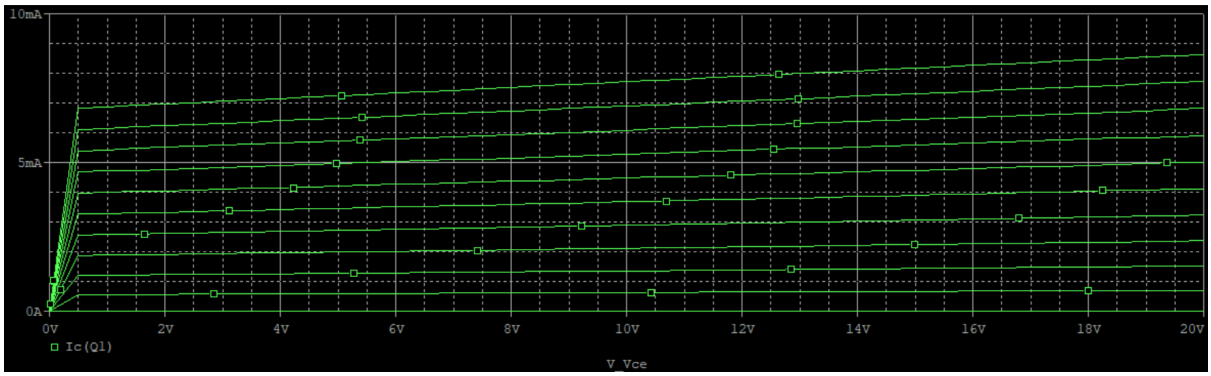


Figure 23: Q2N2222 PSpice Simulation Result

From Figure 23, it can be found that the change between $I_C$ is around 0.7mA and the value between $I_B$ is 4uA. Thus the gain is around 179.

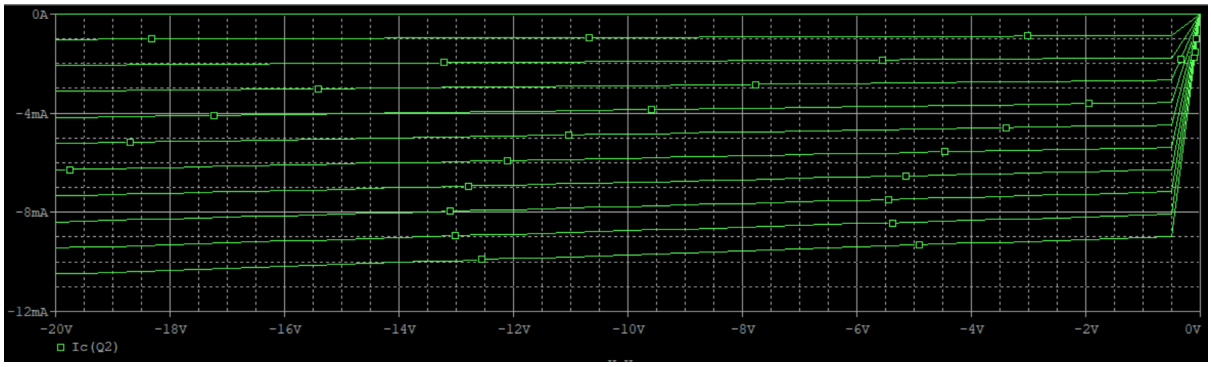


Figure 24: Q2N2907 PSpice Simulation Result

From Figure 23, it can be found that the change between $I_C$ is around 0.9mA and the value between $I_B$ is 4uA. Thus the gain is around 232.

## 3.2 Part II: Achieving the Specification of the Operational Amplifier

### 3.2.1 Task 2

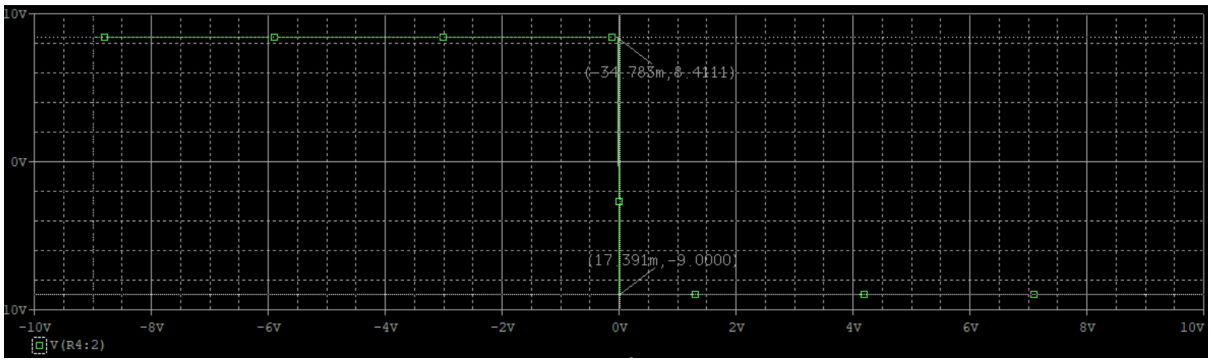


Figure 25: Simulation Result of DC Sweep from -9V to 9V

Figure 25 shows the result of DC Sweep from -9V to 9V. It can be indicated that the effective range is between the voltage of -24.8mV and 17.4mV. After further investigation, the new DC sweep from -125uV to -90uV was set to explore a more accurate useful range.

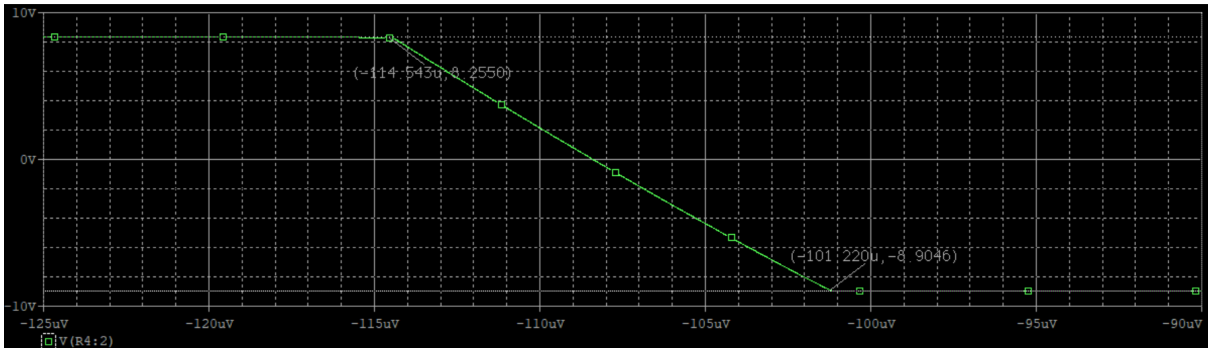


Figure 26: Simulation Result of DC Sweep from -125uV to -90uV

Figure 26 displays the narrow range of the DC Sweep and it can be observed that the more accurate useful range is from -114.5uV to -101.2uV.

### 3.2.2 Task 3

From Figure 26, the voltage can also be obtained from the scope as it shown in Equation 19.

$$A_{ol} = \frac{\Delta V_o}{\Delta V_i} = \frac{-8.9046 - 8.2550}{-101.220u - (-114.543u)} = -1287968.175 \tag{18}$$

### 3.2.3 Task 4

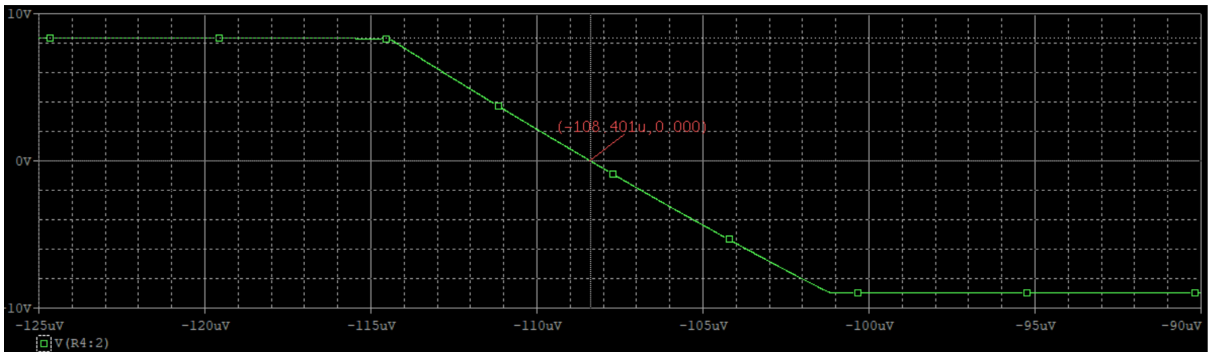


Figure 27: Simulation Result of DC Sweep from -125uV to -90uV with 0V mark

As it shown in Figure 27, at the point that $V_o$ approach 0, the voltage of input is around -108.4uV. This may mean that, a DC offset of -108.4uV is required to balance this op-amp.

### 3.2.4 Task 5

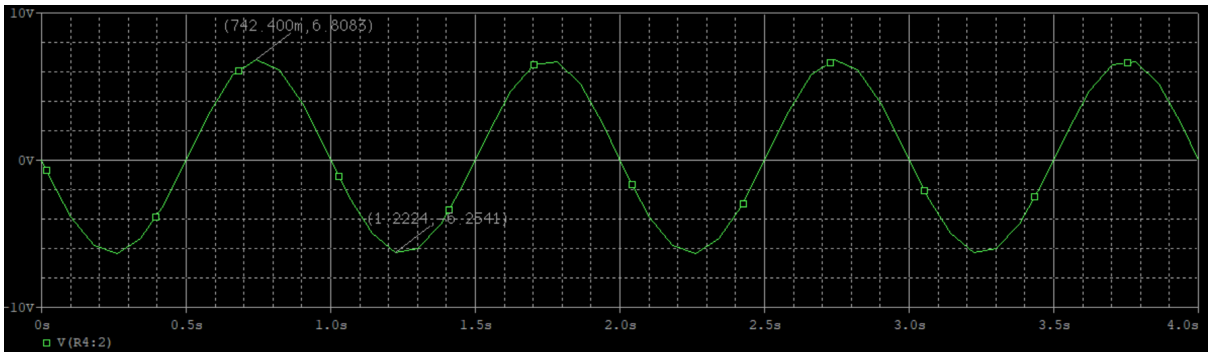


Figure 28: Simulation Result of Transient form 0 to 4s

From Figure 28 of the output voltage, it can be observed concerning the maximum and minimum value of the output voltage. The gain can then be obtained through the following Equation.

$$A_v = \frac{\Delta v_o}{\Delta v_i} = \frac{-6.2541 - 6.8083}{10u} = -1306240 \tag{19}$$

Because the value 1,306,240 is larger than the required 500,000, the design objective was achieved.

### 3.2.5 Task 6

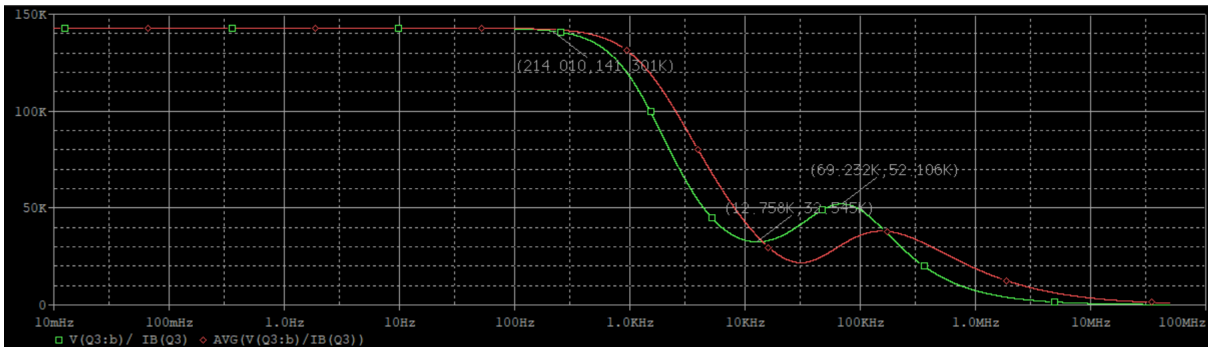


Figure 29: Simulation Result of Input Impedance and its Average with Frequency

Figure 29 displays the simulation result of input impedance and its average value with frequency. It can be observed that for frequency less than 214Hz, the input impedance is about $141k\Omega$. However, after this point, it drops to $32.5k\Omega$ at 12.8kHz then arises to $52.1k\Omega$ at 69.2kHz and finally drops to 0 at 10MHz.

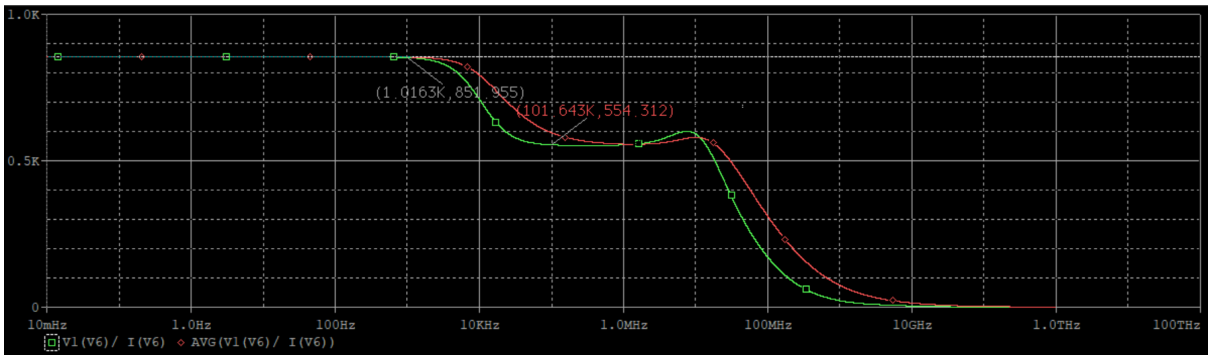


Figure 30: Simulation Result of Output Impedance and its Average with Frequency

Figure 30 shows the simulation result of the output impedance against frequency. It can be noticed that the output impedance remains 852Ω before 1kHz. After that, it decrease for about 300Ω in 99KHz. From 100kHz to 1MHz, the output impedance is flat at about 550Ω. In the frequency of more than 1MHz to 10GHz, the output impedance gradually decreases from 0.5kΩ to 0.

### 3.2.6 Task 7

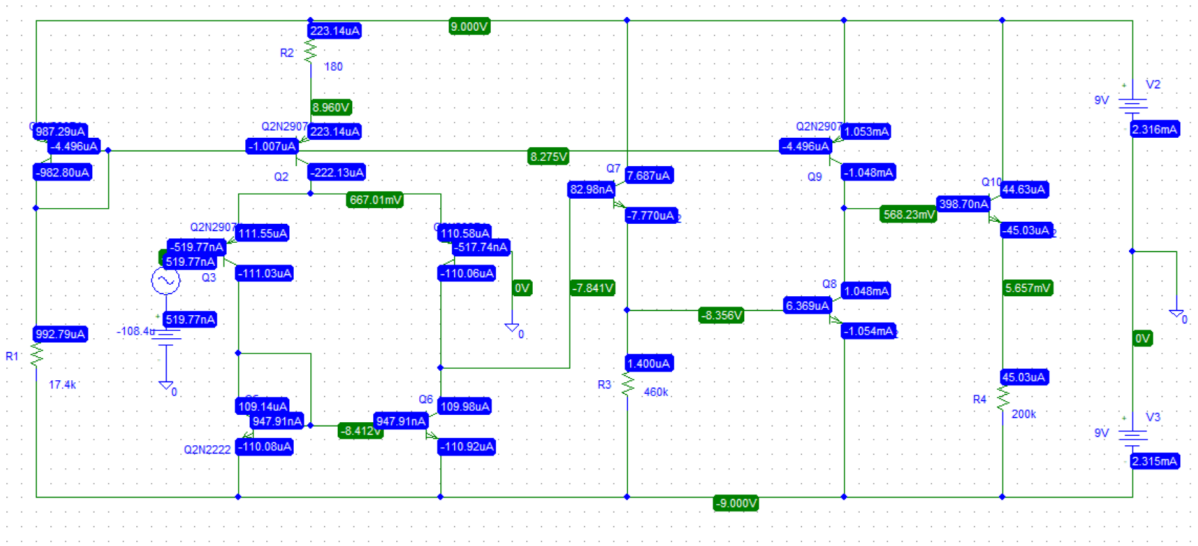


Figure 31: Schematic Simulation with Current and Voltage Display

Figure 31 presents the static current and voltage consumption of the designed op-amp circuit. It can be observed that the DC output voltage is 5.657mV and which is nearly 0 of the specifications.

It can also be indicated from the Figure 31 that the total current consumption is about 2.316mA which is smaller than the required 5mA.

## 3.3 Part III: Obtaining the Frequency Response of the Designed Amplifier

### 3.3.1 Task 1

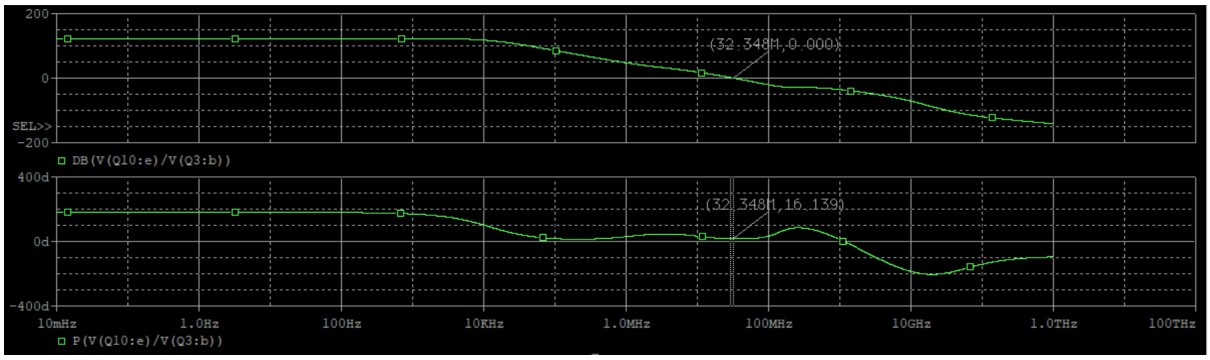


Figure 32: Bode Plots of Gain and Phase

The upper part of Figure 32 shows the plot of gain curve while the lower part displays phase curve. It can be indicated that when the gain is 0dB, the frequency is 32.3MHz. At this frequency, the phase is approximate 16.139d which is much greater than -180d thus it can be inducted that this system is stable.

From Figure 32, the bandwidth of this op-amp could also be inferred. At frequency that less than 10kHz, the gain flat and is about 122.4dB. Therefore, the bandwidth is the frequency range that gain larger than $122.4 - 3 = 119.4dB$. This bandwidth range can be found to be about 0 to 7.7kHz.

### 3.3.2 Task 2

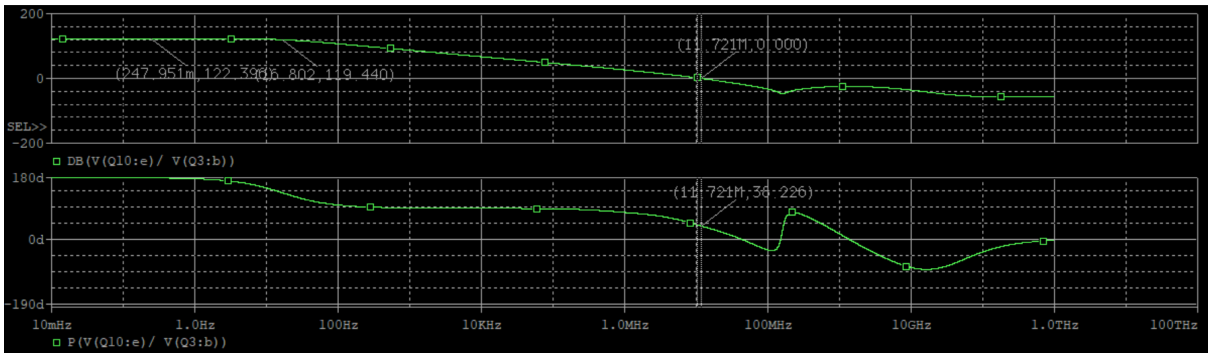


Figure 33: Bode Plots of Gain and Phase with Phase Compensating Capacitor

The upper part of Figure 33 shows the gain plot and the lower shows the phase chart in the case with a phase compensating capacitor. It can be observed that at the frequency that the gain equals 0dB, which is 11.7MHz, the value of the phase is 38.226d, which is larger than the 16.139d in the last task. This may mean that comparing with the situation without a phase compensating capacitor, this capacitor could increase the system stability of this op-amp considerably.

Besides, it can also be observed that the effective bandwidth had decreased to 68.8Hz in the condition with a phase compensating capacitor.

## 3.4 Bonus Part: Response to Common-Mode Signal

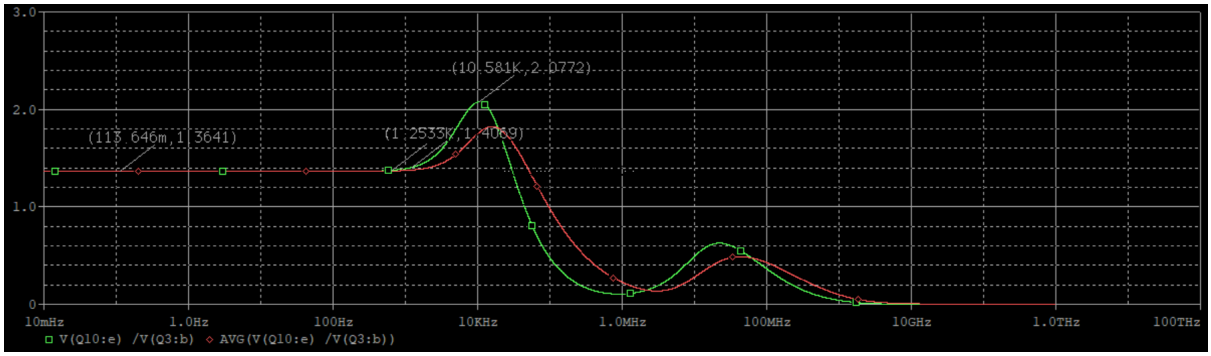


Figure 34: Gain Plot against Frequency of Common-Mode Signal

Figure 34 shows a plot of the voltage gain of common-mode signal. To reality, the common-mode gain of the op-amp is expected to be as small as possible. As it shown in Figure 34, before 1.25kHz, the gain of common-mode signal is about 1.37. From 1.25kHz to 10.5kHz, the gain gradually increases up to the gain of 2. After 10.5kHz, the common-mode gain decreases

effectively down to nearly 0 at 1MHz. After that, the gain slightly increases to 0.6 and eventually decreases to 0.

It can be indicated that the common-mode gain is less than 2 in most case, which is much less that the corresponding differential-mode gain which is about 1.3M.

In addition, it can also be inferred that the noise from common-mode signal could have a peak at around 10kHz because the common-mode gain is highest at this frequency.

### 3.5 Design Specifications Table

Table 4: Design Specifications Table

| Parameter | Specification | Value | Comment |
|---|---|---|---|
| Differential input impedance | $\geq 100k$ | 141k | This value is designed as assumption which is 140k. It satisfies the requirement of greater than 100k. |
| Open loop voltage gain | $\geq 500,000$ | 1,287,968 | The gain was measured in section 3.2.3 and 3.2.5. It is much greater than the required 500,000. |
| Output impedance | $\leq 1k$ | 852 | This value is similar to the assumed 800. It is less than 1k thus meet the specification. |
| DC output voltage | $\approx 0V$ | 5.66mV | This value is around 0 compared with the level of output AC voltage. Therefore, it satisfies the request. |
| DC offset voltage | None given | -108.4uV | This value was obtained in section 3.2.2. |
| Frequency response | Down to DC (0Hz) | 0-7.7kHz | The bandwidth of frequency response is from 0 to 7.7kHz thus meet the specification. |
| Total current consumption | $\leq 5mA$ | 2.316mA | The total circuit consumption is 2.316mA which is smaller than the required value. This value is measured in section 3.2.7. |
| Bandwidth with compensation capacitor | None given | 0-66.8Hz | In section 3.3.2, the bandwidth of the op-amp with compensation capacitor was measured. The value is around 66.8Hz which is much smaller than the condition without a capacitor. |

# 4 Discussion and Conclusion

## 4.1 General Question

### 4.1.1 Answer to Ques 5.a

From the schematic in the above section, it could be easily identified that this op-amp is an open-loop system. Therefore, the value of gain or phase margin could indicate the system stability.

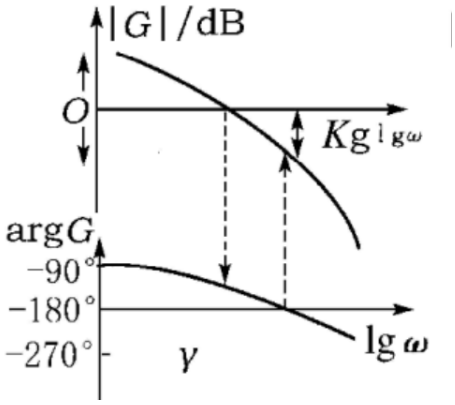


Figure 35: Stable System

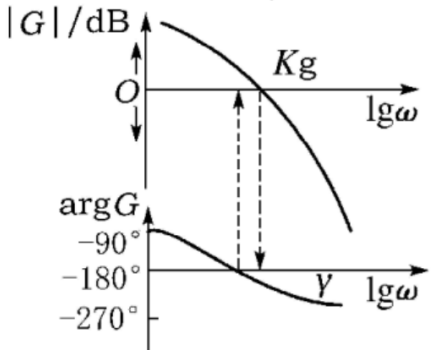


Figure 36: Unstable System

Figure 35 shows a plot of gain and phase of a stable system. It can be observed that at the frequency that the gain equals 0 dB, the value of phase is larger than -180d. However, for a unstable system shown in Figure 36, at the frequency that gain equals 0 dB, the value of phase is less than -180d. From this, it could also be inferred that the greater the phase margin, the distance that the point is greater than -180d, the system would be more stable.

Therefore, according to the result in section 3.3.1 where the phase margin is 16.139d above -180d, it can be indicated that this open-loop system is table at this state.

### 4.1.2 Answer to Ques 5.b

By observing the result in section 3.3.2, it can be acquired that the phase margin for the case with phase compensating capacitor is around 38.226d, which is larger than the 16.139d in the case without a capacitor. This may indicate that the system with compensating capacitor could increase the stability of system.

In addition, it can also be noticed that after add a compensating capacitor, the bandwidth of op-amp is effectively decreased from 7.7KHz to 66.8Hz.

One explanation for this is that the addition of phase compensating capacitor could effectively short circuit the high-frequency signal this skip the CE amplifier. This gives rise to the shorten of delay for high frequency signal to go through the whole op-amp, which increase the phase margin and increase the system stability. However, since a little low frequency could also go through the capacitor to skip the CE amplifier, the bandwidth of low frequency signal could be significantly decreased.

Overall, the purpose of the phase compensating capacitor is to depress the influence of high frequency noise thus improve the overall system stability.

## 4.2 Error Analysis

### 4.2.1 Difference between Assumed and simulated $R_{out}$

It can be noticed at the beginning of the calculation, the output impedance $R_{out}$ was assumed to be 800Ω. However, after the simulation in section 3.2.6, it was found that the measure output impedance was 852Ω.

One reason for this is that during the calculation, some of the calculating result especially the value of four resistors were approximate for the purpose of component purchase convenience. For example, the value of 184.4 was approximate to be 180.

The other possible error is that the adoptive known value in Table 2 are not exactly the same as the simulation model in PSpice.

### 4.2.2 Difference between Assumed and simulated $R_{in}$

From the above section, it can be noticed that the simulated value $R_{in}$ which was $141k\Omega$ is different from the value assumed which is $140k\Omega$. There are several explanation for this.

Firstly, the approximation error could be considered similar to the error in calculating $R_{out}$. Then, the bias from the assumed known parameters could also be wrong.

Additionally, the main reason for this is because that in the calculation process, some of the parameters that is relevant to the input resistance were represented and covered by the assumed $I_{R1}$ which was 1mA. In other words, some information in the assumption of $I_{R1}$ indicates the actual value of $R_{in}$.

### 4.2.3 Difference between the Two Gain from Section 3.2.3 and 3.2.5

It can be pointed that through the two gain measured in section 3.2.3 and section 3.2.5 were both voltage gain for the same op-amp, their value are not the same.

One reason is that the error was caused by the error of the simulation. For example, the step value could be different for this two simulation. Besides, the different methods of measurement may also give rise to the difference in result.

The other possible explanation is that because the result in section 3.2.3 was observed on a DC sweep, while the result of section 3.2.5 was simulated by AC source, the frequency of AC signal might influence the result to some extant.

### 4.2.4 Difference between the Calculated and Actual Value of Four Resistors

It can be noticed that the value of four resisters in the schematic were different from the calculated value. This error was caused with caution for the purpose to convenient the components selection. This is because that not all of the resistors with special value could be found in market, thus the value need to be slightly change to meet the regular types that are popular on supplier's website.

## 4.3 Limitation and Suggestions

It can be noticed that the value of $\beta_{npn}$ and $\beta_{pnp}$ were simulated from the testing circuit in 3.1. Due to the accuracy of calculation, the accuracy of there known value could be further precise. Inevitably, this designed op-amp was simulated with PSpice but not being implemented as actual circuit. Since the simulation could only approach the reality with some errors, actual works could be done to further investigate the feasibility of this op-amp.

In addition, this op-amp could only perfectly amplify the signal that less than 7.7kHz. This bandwidth could be further extend to make this op-amp more generally utilized. For example, the bandwidth could extend to 1MHz without significant change on the system stability. For high frequency usage, the EMC could also be considered when designing to prevent EMI. Especially when this op-amp was designed for certain RF circuit. This measure could make this product more stable in more conditions.

## 4.4 Conclusion

To conclude, in this experiment, an op-amp meet all of the specifications was designed and simulated to measure a set of parameters. This op-amp has a differential input impedance of 141k$\Omega$ and a output impedance of 852$\Omega$ while it needs a 9V $V_{CC}$ and -9V $V_{EE}$ DC supply and has an open-loop voltage gain of 1,287,968. The total current consumption of this op-amp is 2.316mA and the frequency bandwidth is 7.7kHz. This op-amp was designed from the assumption of $R_{in}$ and $R_{out}$ with necessary known parameters. With differential input, differential signal could be amplifier for twice while the common-mode noise will be eliminated. In addition, the stability of the system was investigated and improvement such as compensation capacitor was explored.

## References


[1] S HallT DowrickA Al-AtabyM Lopez-Benitez, "Experiment 5 - design of and operational amplifier using pspice," https://vital.liv.ac.uk/bbcswebdav/pid-2008628-dt-content-rid-13997554_1/xid-13997554_1, University of Liverpool, 2020.

[2] P. Vizmuller, *RF design guide: systems, circuits, and equations.* Artech House, 1995.

[3] S. Hall, "Exp 5 pre-lab test images," [EB/OL], https://vital.liv.ac.uk/bbcswebdav/pid-2008627-dt-content-rid-11300831_1/xid-11300831_1 Accessed May 6, 2020.